Australia's National Science Agency

Applications of an RFSoC based Digitiser Platform to Digital Receiver Systems

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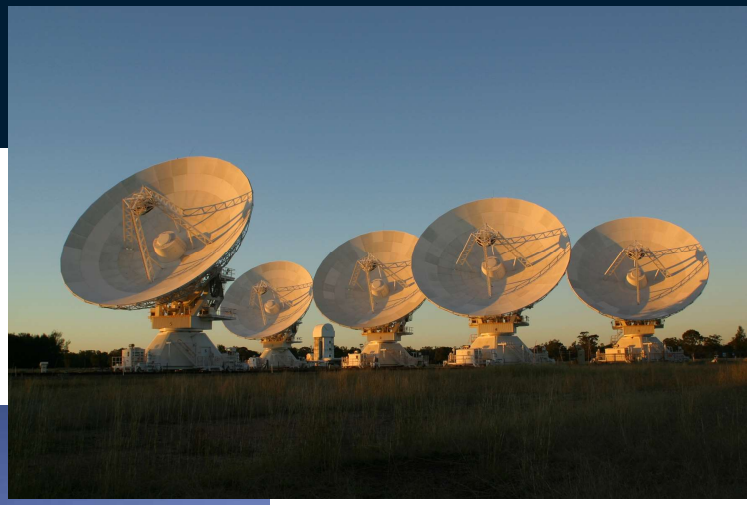
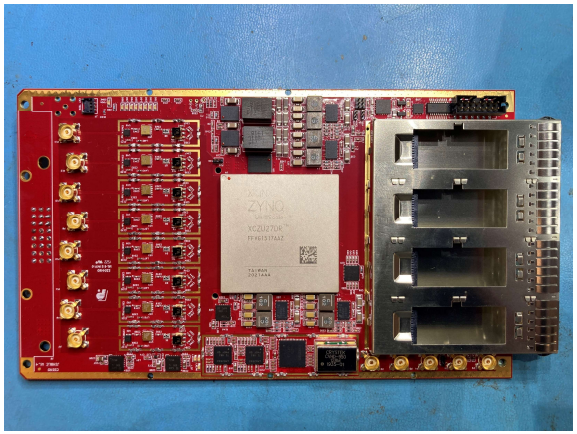




A common DR platform for multiple current/future CASS instruments - “Jimble”

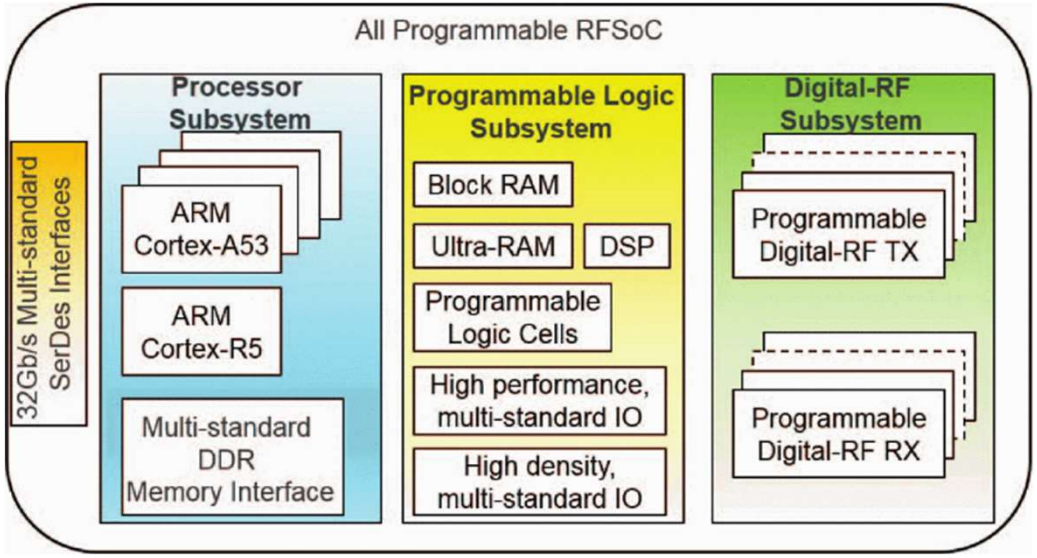
- Several new systems under development and old systems in need of upgrade in immediate future
  - CryoPAF
  - BIGCAT – Upgrade to aging AT 6 element 22m interferometer backend
  - UWL – Upgrade of Parkes 0.7- 4GHz UWL backend
  - UWH – Future enhancement of UWB coverage to ~24 GHz
  - Spectrum monitoring, EOR receiver and other specialty projects

- A single platform being developed to leverage design reuse and firmware/ software reuse

- All projects use a common signal processing architecture and control design

- Modern systems moving to digitising near focus and RF to ‘packets’ architecture

Xilinx RFSoC Platform. An FPGA plus ADC/DACs and Processors



Four major parts to RFSOC:

- **Digital-RF subsystem (ADC/DAC)**
- **Programmable logic (FPGA core fabric)**
- **Processor System (ARM Cortex)**
- **SerDes interfaces (high speed serial IO)**

Powerful combination of four technologies in one.

High integration, performance and cost savings

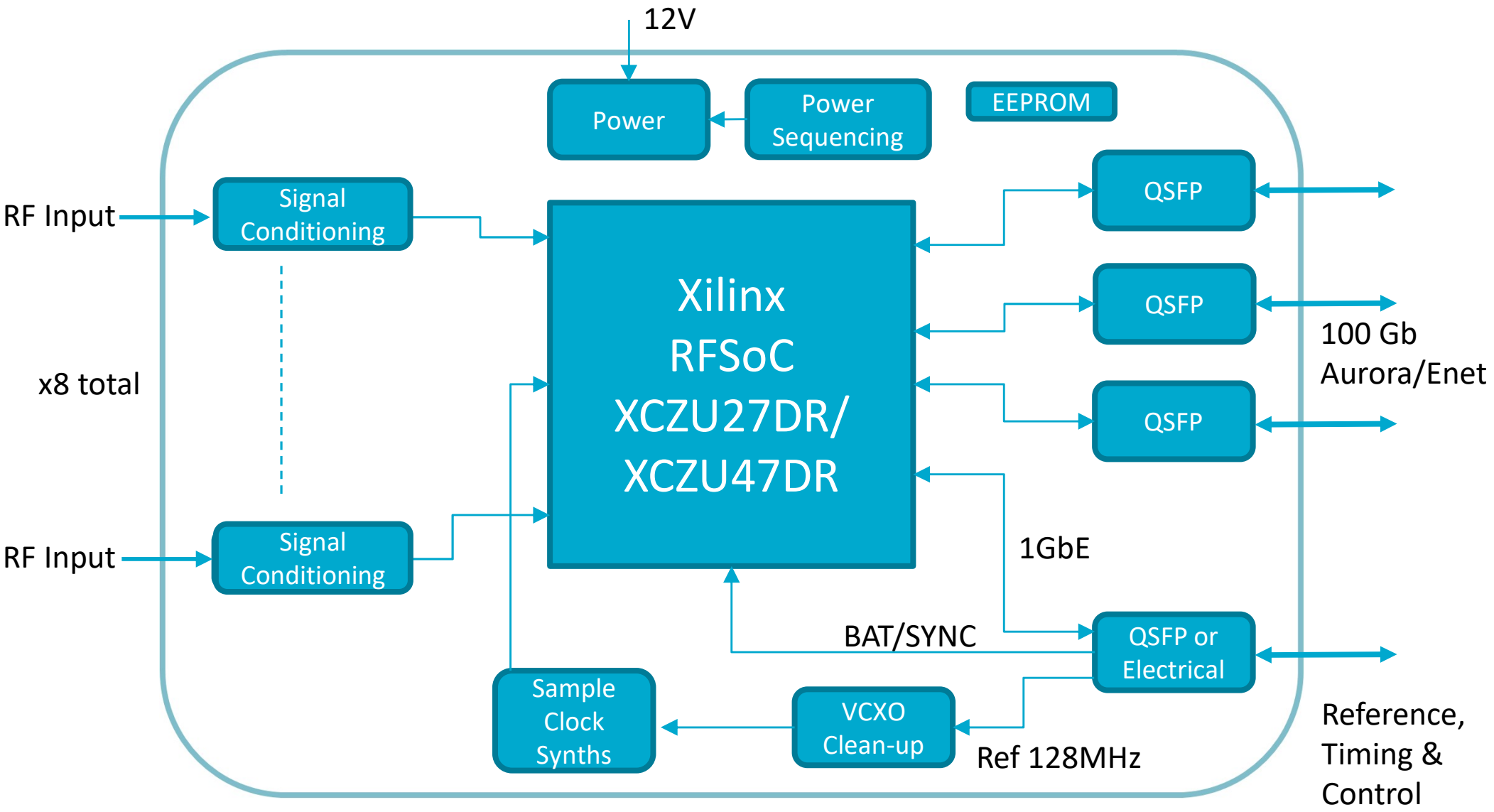
Gen-1
- 16 x 12 bit 2GSPS ADCs
- **8 x 12 bit 4GSPS ADCs**

Gen-3
- 16 x 14 bit 2.5GSPS ADCs
- **8 x 14 bit 5GSPS ADCs**

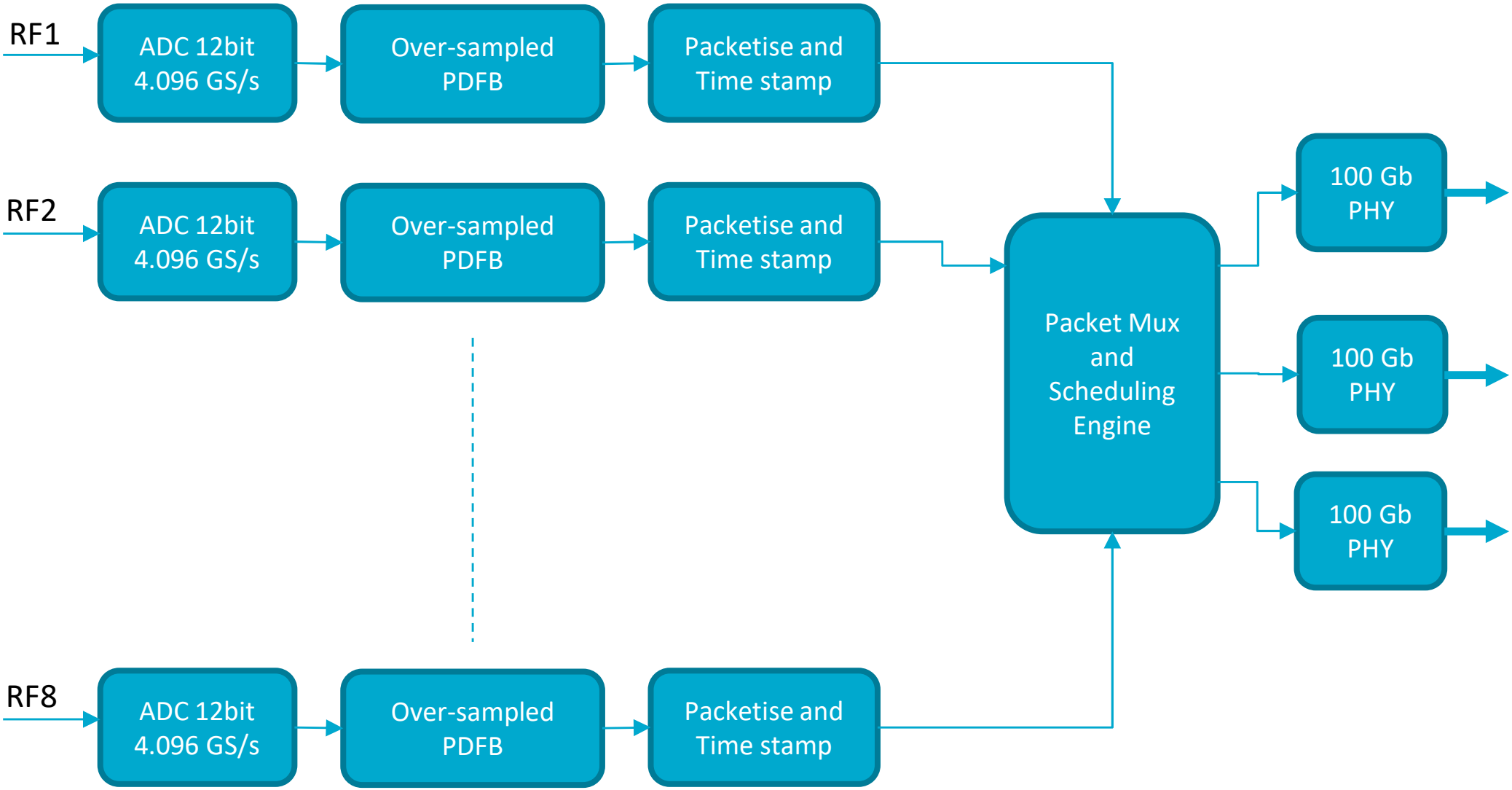
“Jimble” Design Philosophy

- Simple – remote ADC/Packetiser/Transmitter applications
  - Small but powerful like namesake
- Ultra Low EMI – attention to EMI and no local DRAM (On Chip Mem only)
- Reusable in other applications – 3U 100x170mm reusable form factor
- Data/Timing/Reference/Control interfaces – Fully optical (optional electrical)
- Only electrical inputs are RF and power
- Command and control 1/10 GbE

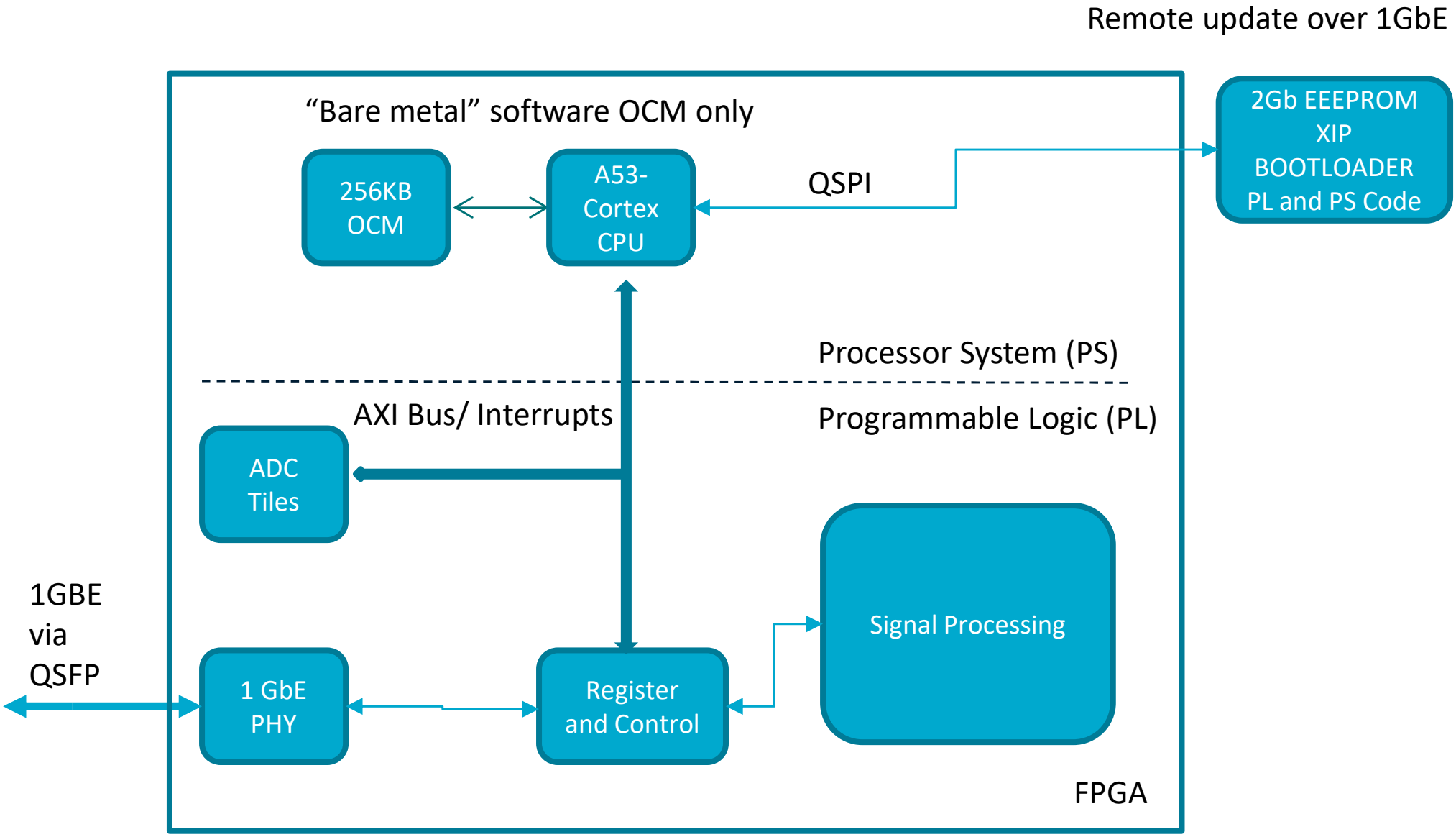
“Jimble” Module Hardware Overview



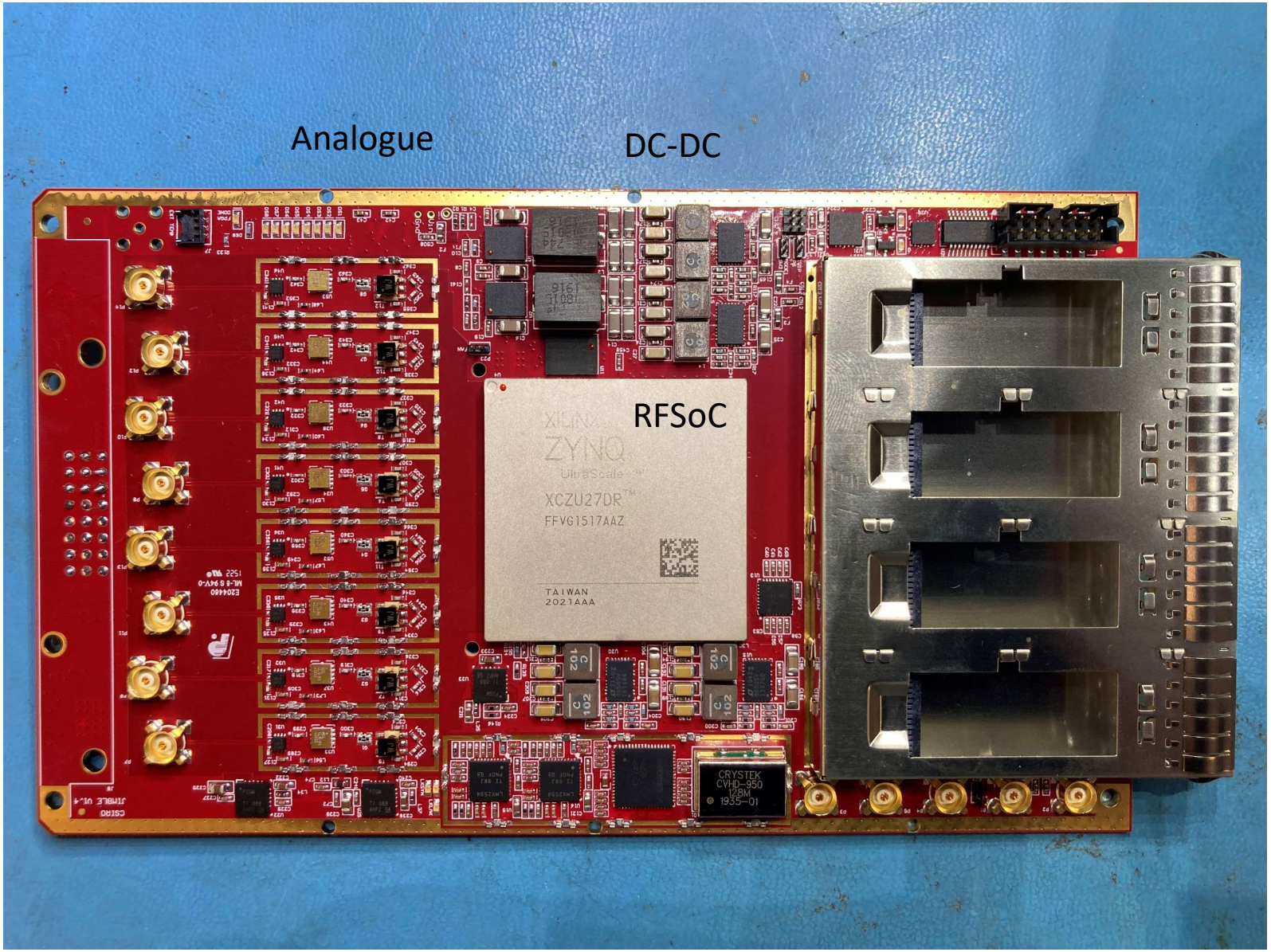
“Jimble” Module Typical Signal Processing



“Jimble” Module Control Architecture



Board Form Factor and Layout



Jimble Module Spec Sheet

Parameter	
RF Inputs	8
Input operating frequency	10MHz - 4GHz (6GHz 47DR)
ADC resolution	12 bits (27DR) / 14bits (47DR)
Max sample rate	4.096 GS/s (27DR) 5.0 GS/s (47DR)
SNR	58 dB / 9.5 enob
Operating headroom	36 dB
RFSoC	XCZU27DR1517 / XCZU47DR1517
- DSP48	4272
- BRAM	38 Mb
Sample Data IO	3 x 100 GbE QSFP28
Control/Reference/Timing	QSFP+ or electrical
Output packet format	CODIFF
Size	100mm x 170mm
Supply	12V
Power	100W max

“Irukandji” Clock, Sync and Control for “Jimble”

Overview

Provide reference clock, synchronisation signal, calibration signal and ethernet control to each of the RFSoC based boards over a single optical cable connection

Allow synchronisation of the ~200 ADCs, signal processing and time stamping of streamed packet data for later processing in the beamformer etc.

Distribute over star fanout network so one QSFP optical connection to each slave RFSoC board or another slave Irukandji

(Up to 32 slaves)

Flexible enough to synchronise to station 10MHz and 1 Hz, or BAT (PWM or ME) and high frequency reference (128MHz, 125MHz, 32 MHz etc)

IrukandJi architecture

REFCLK - 128MHz
SYNC – ME BAT
CAL
ETHERNET – 1GbE

REF 5/10/16/128 MHz

DIFF BAT

SYNC

1PPS

CONTROL (ETH, USB)

ETH
SWITCH

VCXO

PLL

RES

FPGA

REF
1:32

SYNC
1:32

CAL
1:32

32:32

8
QSFP+

32 QSFP+

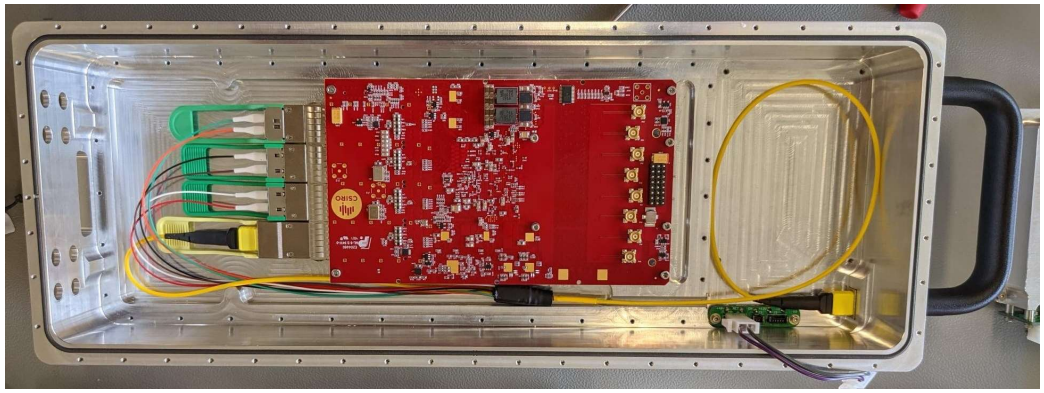
FRONT

1U x 19in subrack

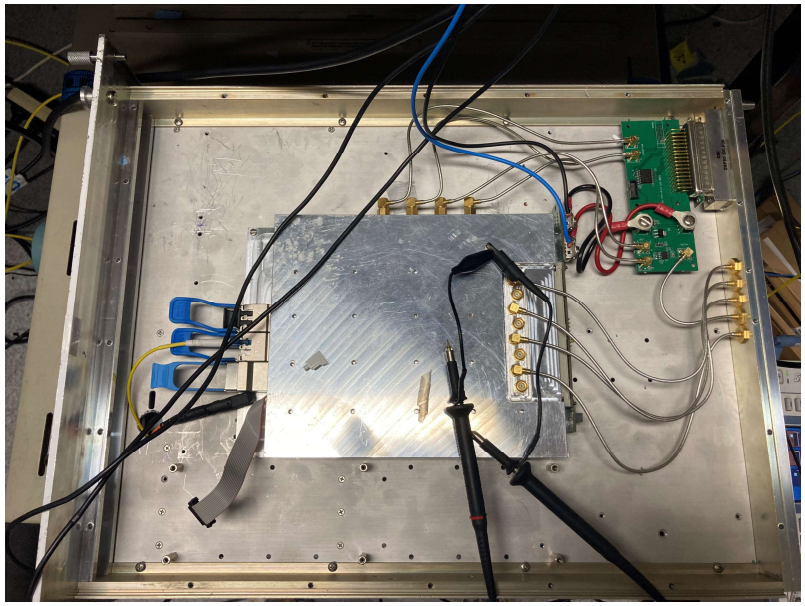
Irukandji

Jimble packaging – application dependent

But must provide appropriate thermal management and RFI shielding



CryoPAF WEM – see Peter R talk
Excellent thermal and RFI performance



BIGCAT prototype antenna module

Jimble Verification – includes

Measured clock jitter after cleanup loop and HF synthesis 88fs @ 4.096 GHz

SNR of ADC sampled data 58 dB

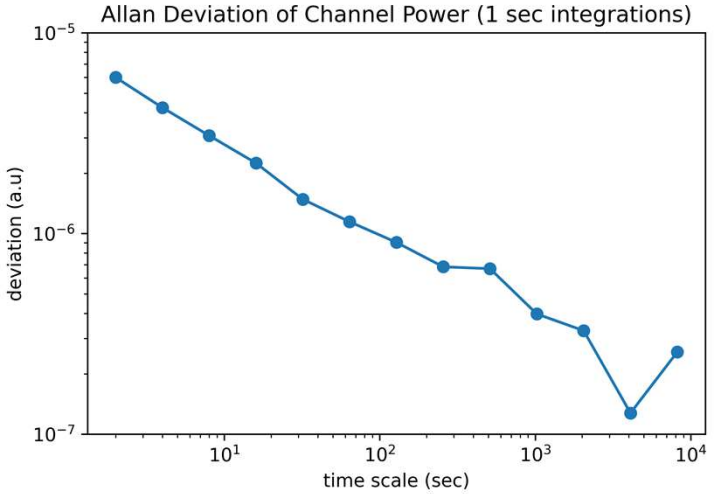
Interleaving artifacts < -91 dBc – discrete spurs at nFs/4 visible above noise floor

Adjacent channel RF isolation max -67 dBc

Flat bandpass response within 3 db to 4 GHz

100 Gb data transmission at 100% utilisation through board, QSFP, 200m fibre, 6 connectors gives 0 bit errors in a week (BER < 7.4e-17)

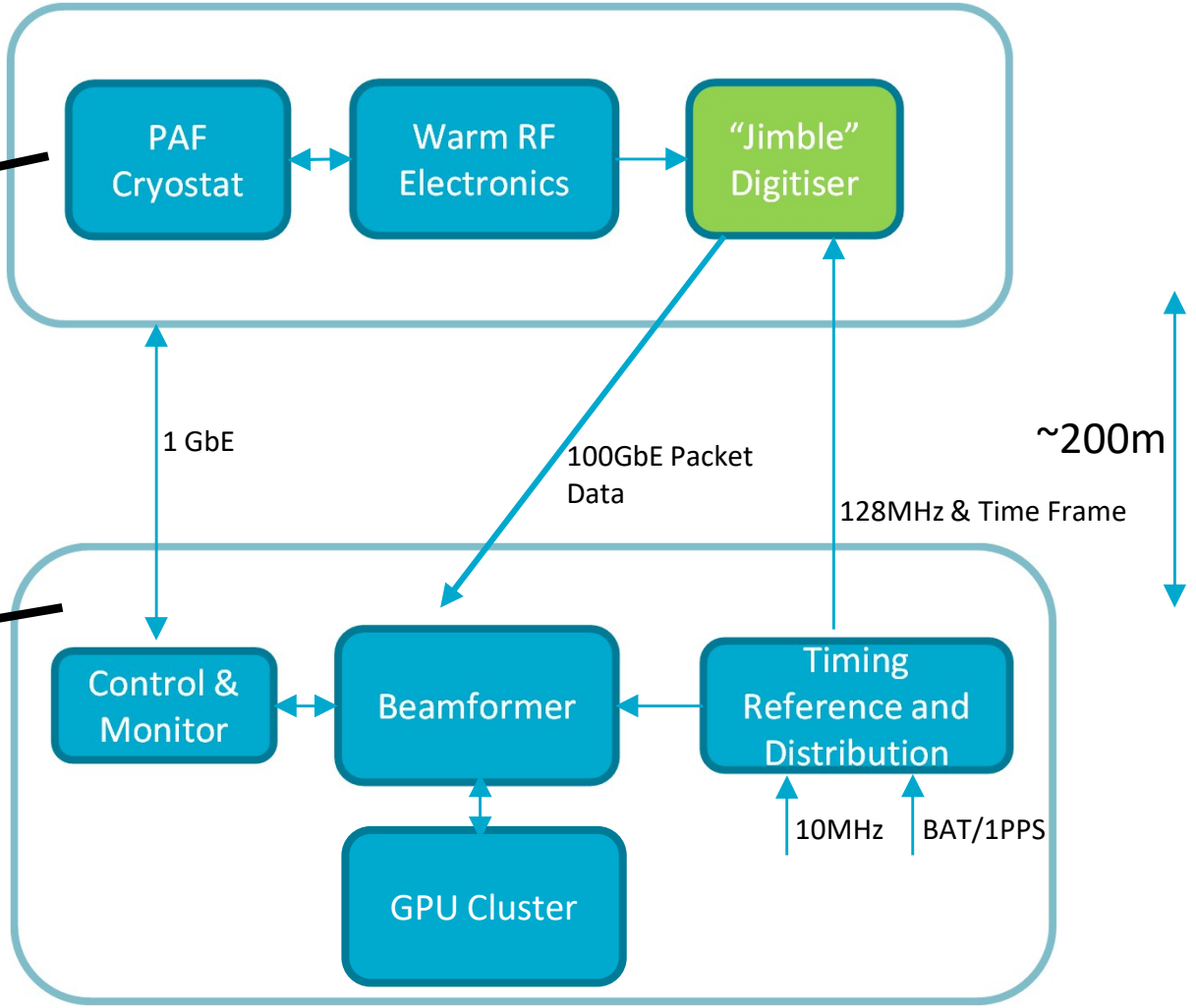
Stability of spectral channel power - insulated noise source gives Allan deviation turn over beyond 3 hours



Design operates at full expected load power

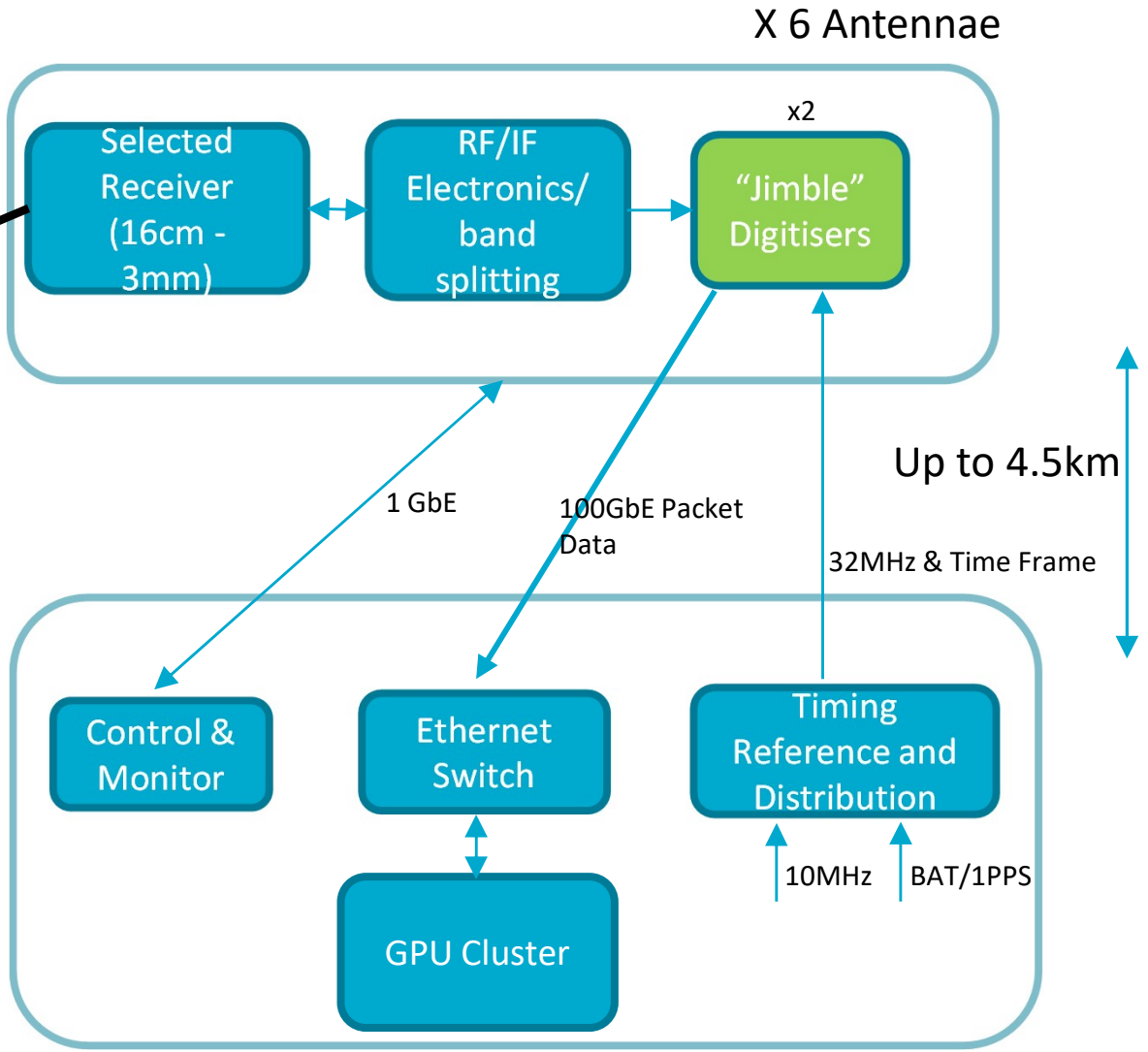
FPGA junction temp <60 deg (Peter R WEM)

CryoPAF Application



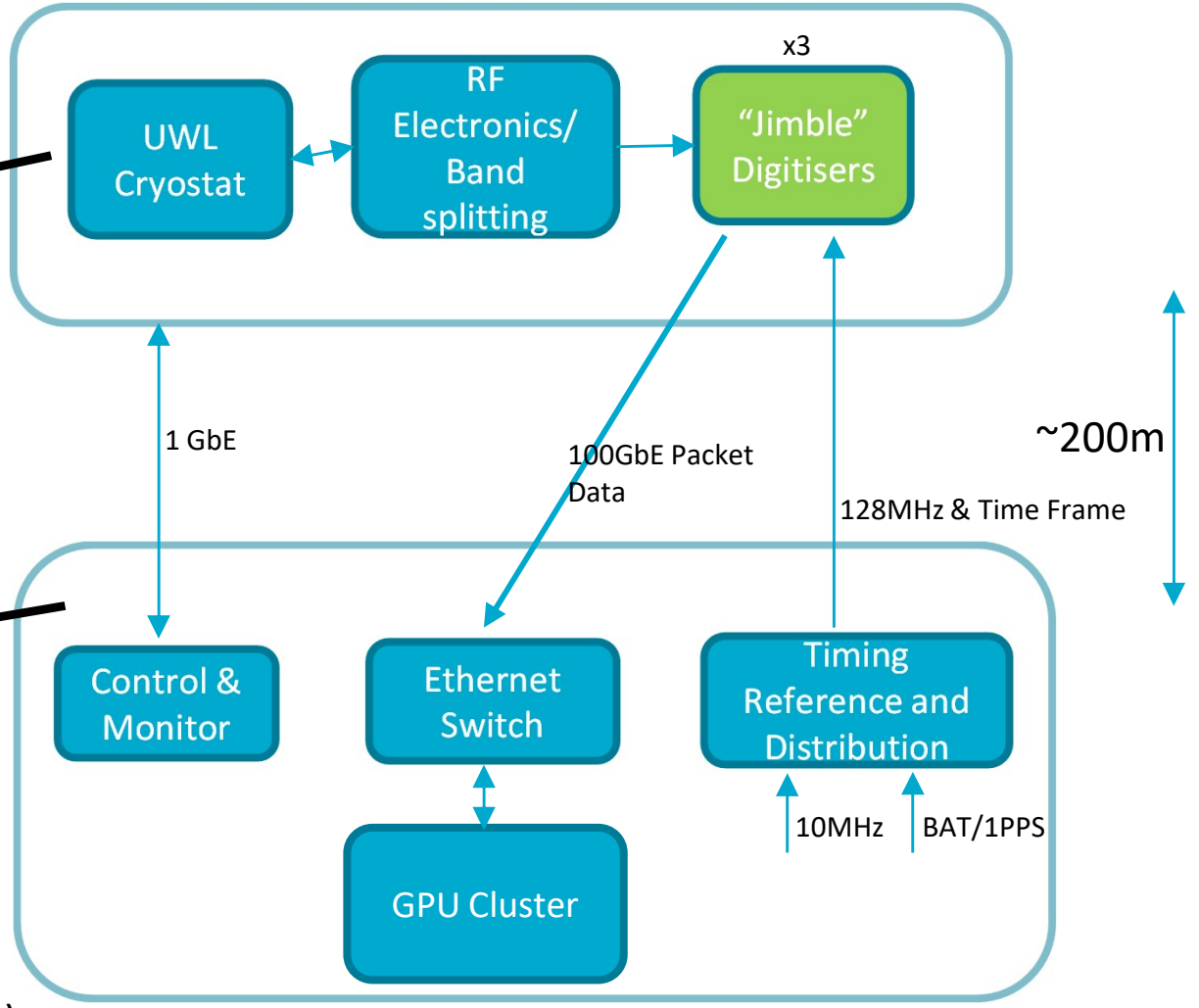
Freq coverage: 700-1950MHz
Inst. BW. ~600 MHz
1.6 MHz OS Channels from Jimble
196 Elements + Cal/RFI

BIGCAT – (Broadband Integrated GPU Correlator for ATCA Telescope) – Application



Freq coverage: 16cm – 3mm in bands
128MHz OS Channels from Jimble
4 IF bands
Dual polarisation
Inst. BW. 2048 MHz per IF
Total 8 GHz dual pol

UWL Application



Freq coverage: 700-4032MHz (UWH ~24GHz)
128MHz OS Channels from Jimble
Inst. BW. Full 3328 MHz
Dual polarisation

Summary

An RFSoC based custom digitiser and data transmitter platform “Jimble” was presented

Key features were it’s versatility, reusability in various applications, small form factor and design for EMI quietness.

The application of the developed platform in a selection of current and future system was discussed.

First production run due to commence in a few weeks after final verification tests.

Thank you
Questions

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