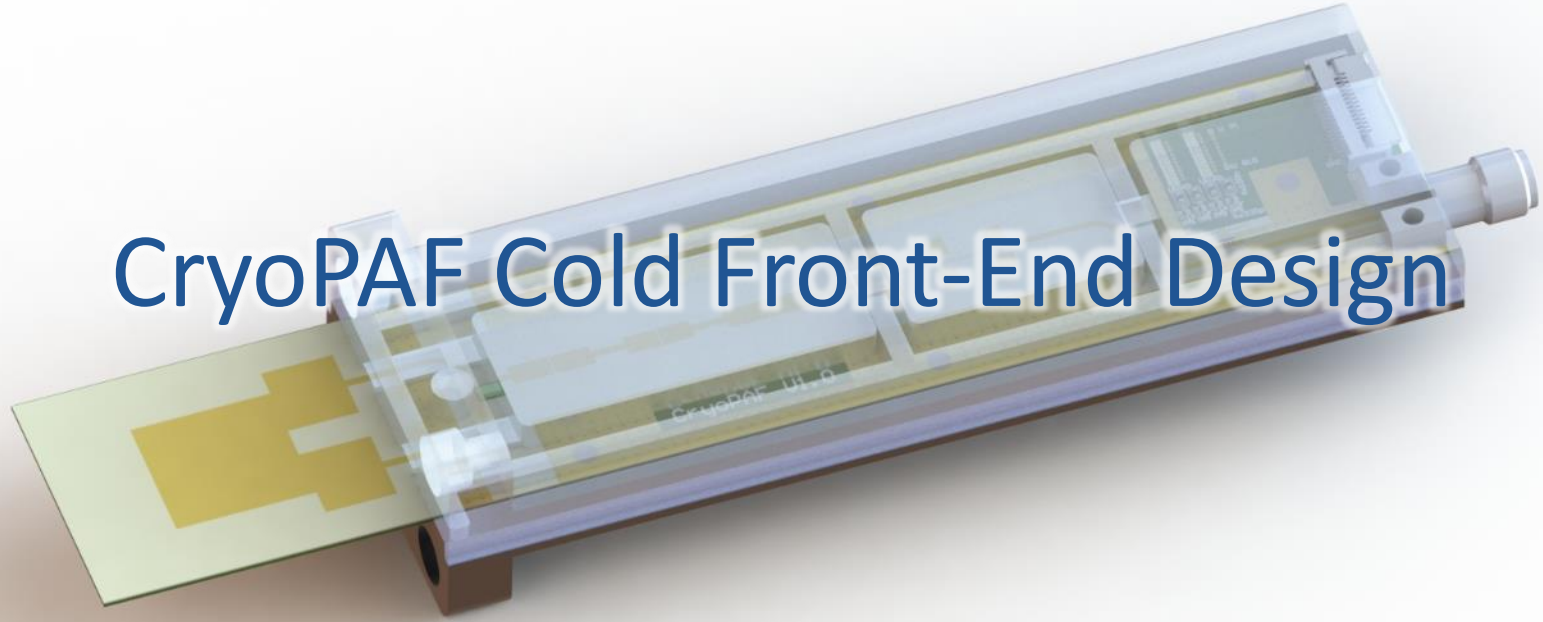
CryoPAF Cold Front-End Design



P. Pütz and M. Mbeutcha, S. Heyminck, C. Kasemann

on behalf of the CryoPAF FE team

Key requirements

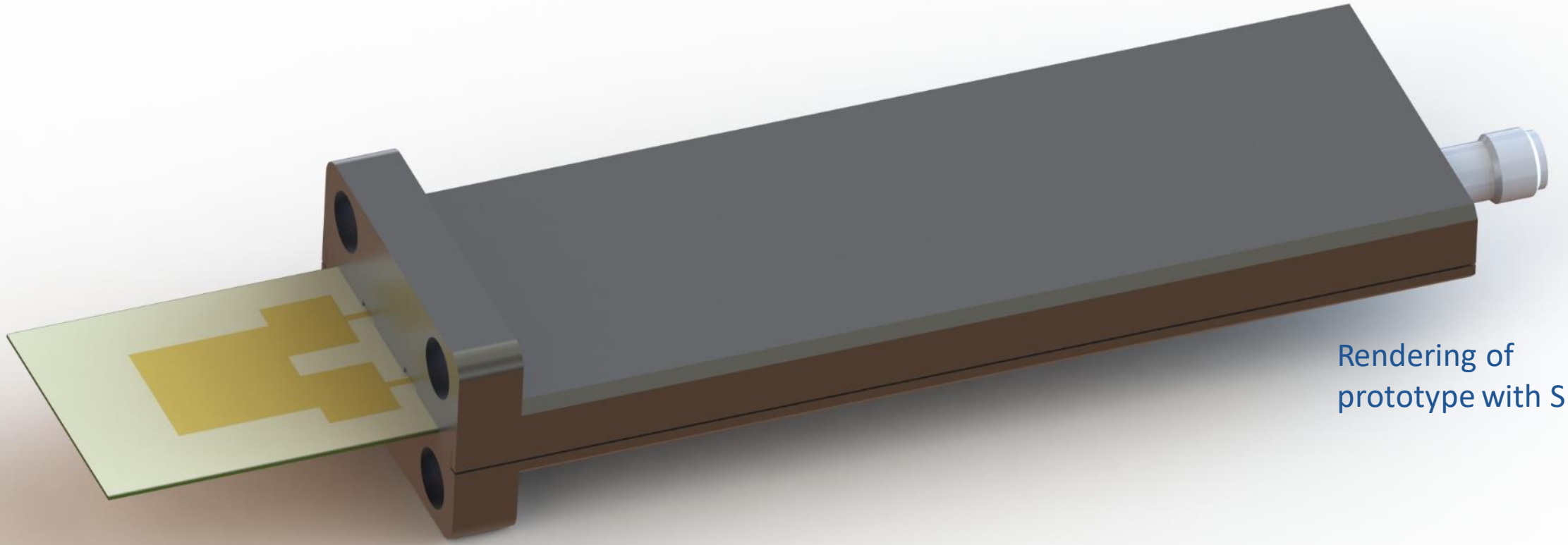
- Scalability of production to hundreds or thousands of cryogenic signal chains
  - 250 pcs. for Effelsberg's 1st generation CryoPAF (2.5 – 4 GHz)
  - For future PAF at higher frequencies: +1 magnitude
  - Explore and qualify suitable SMT and PCB technologies to facilitate automated assembly
- Overall reduction of cryogenic front-end sub-component count
  - Allow for front-end level modularity (maintenance)
  - Simplification of cryogenic FE signal chain
  - Integrate LNA (package) with cryogenic FE circuits (antenna, balun, BPF)
  - Utilise COTS components were applicable

Baseline design

cryoPAF

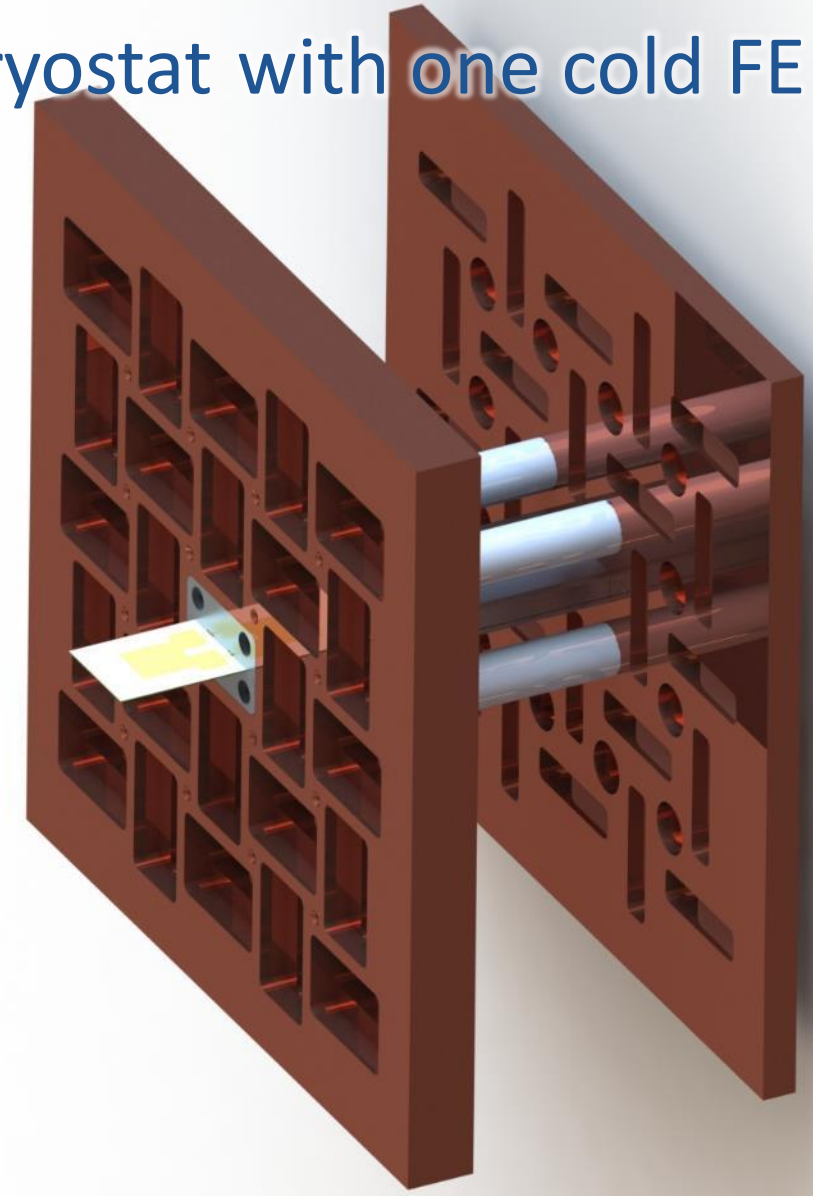
- “plug-in card” concept
  - module per signal chain containing whole cold FE circuitry (x250)
  - Single common PCB for cryogenic signal chain incl. antenna, balun, filter, LNA, DC bias components and DC/RF connectors
  - Clamshell housing
  - Blind-mating COTS connectors
- PCB technology
  - Width = 24.5 mm (upper limit set by antenna element spacing)
  - 10 mil Astra MT77 low loss dielectric
  - PCB internal grounding scheme for MMIC pad to MSL
- Components
  - MMIC 2 – 4 GHz from IAF
  - SMD balun
  - Cost-effective DC connector

CryoPAF cold FE module



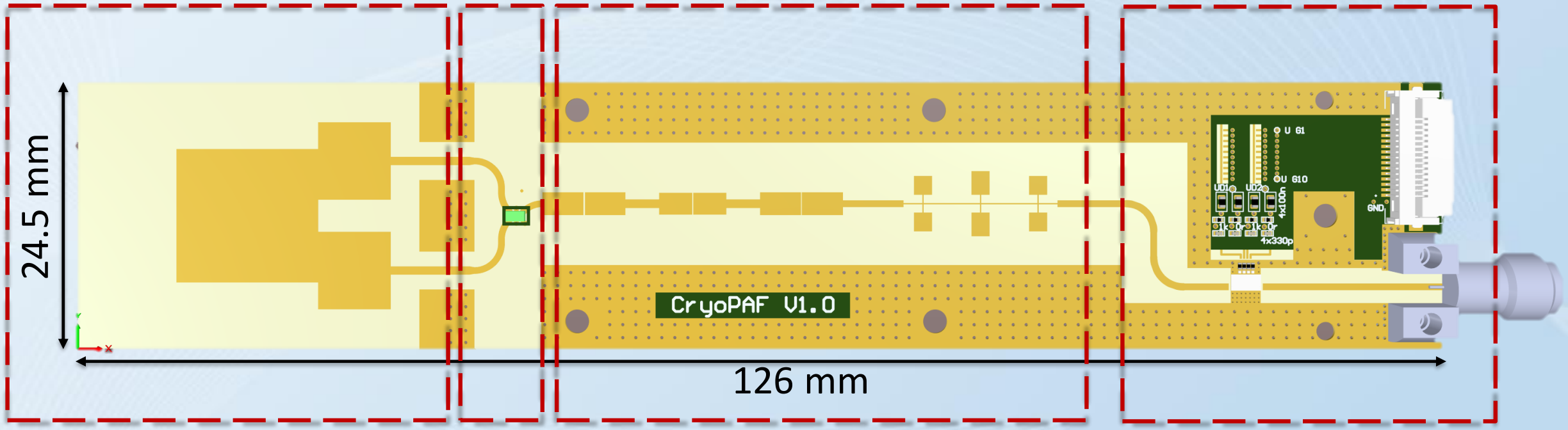
Rendering of
prototype with SMA

CryoPAF cryostat with one cold FE module



Cold FE PCB baseline design

cryoPAF



Antenna | Balun | BPF | LNA with DC bias

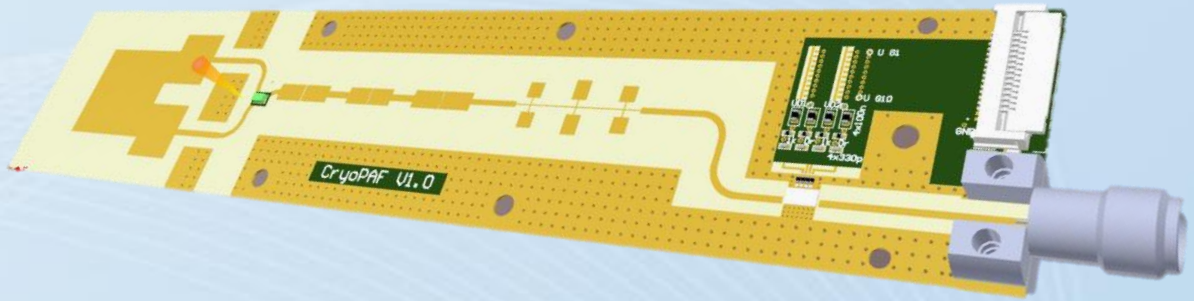
Prototype V1

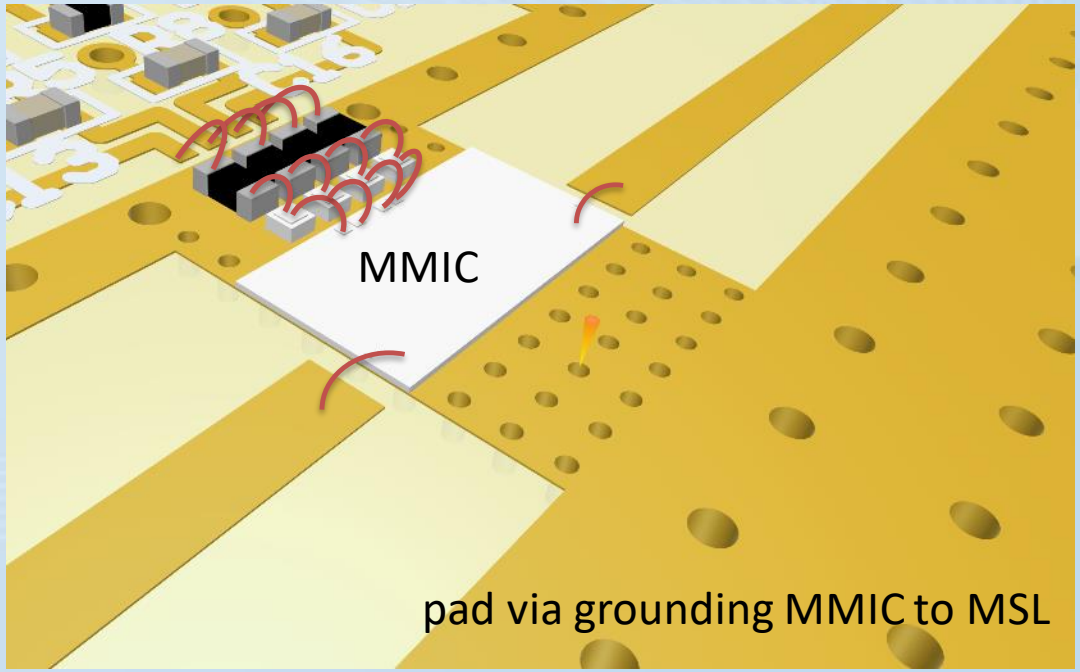
Development roadmap

- Identify suitable PCB technology
  - Initial prototyping with PCB technology demonstrators
- Design clamshell housing
  - Antenna feedthrough and PCB grounded to housing with springs (RFI mitigation)
  - PCB antenna side floating wrt. housing, PCB fixed at connector end
- Connectors
  - DC: multi-pin right-angle SMD type, evaluate COTS
  - RF out: SMP or smaller
- RF and cryo-mechanical testing
  - PCB technology for LNA
  - Cryogenic evaluation of SMD balun (presented by M. Beutcha)
- Automated PCB assembly
- **Design of prototype of cold FE PCB**

Cold FE PCB prototype

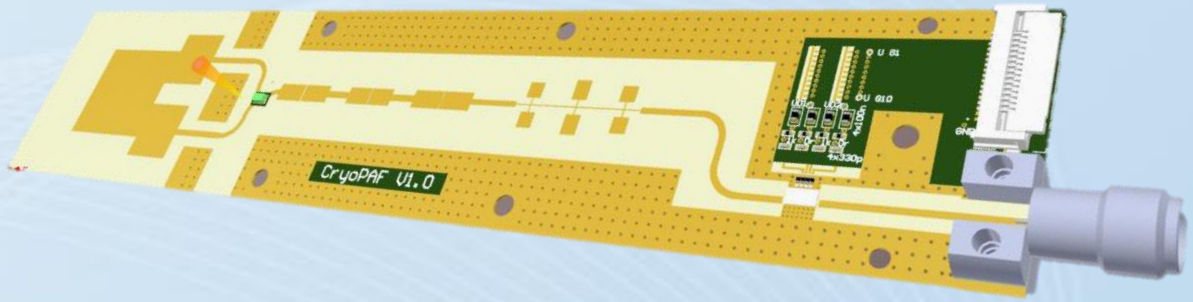
- Cryo-mechanical and RF performance evaluation
- Connectorized sub-circuits
- Connectors
  - SMA output
  - FPC/FFC connector for DC
  - Blind-mating on V2 PCB
- pad via grounding MMIC to MSL
- 10 mil MT77 with 2 metallisation layers
- 10x Vg voltage bus from connector
  - SOT with bond wire connection
  - SOT voltage divider will be implemented on V2 of PCB

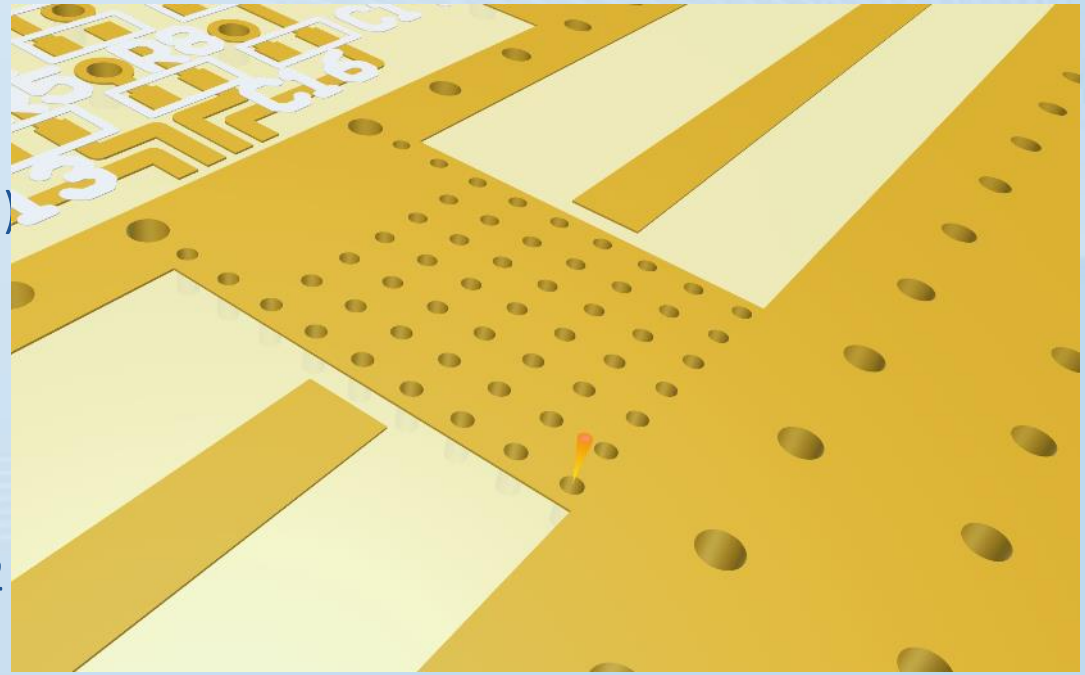




Cold FE PCB prototype

- Cryo-mechanical and RF performance evaluation
- Connectorized sub-circuits in various combinations
- Connectors
  - SMA output
  - FPC/FFC connector for DC
  - Blind-mating on V2 PCB (SMP + board-2-board)
- **pad via grounding MMIC to MSL**
- 10 mil MT77 with 2 metallisation layers
- 10x Vg voltage bus from connector
  - SOT with bond wire connection
  - SOT voltage divider will be implemented on V2 of PCB





MMIC

- MMIC designed and fabricated by our long-term partner Fraunhofer-IAF
  - 3 different designs under evaluation
  - MMIC V2 show more bandwidth and less performance spread
- 2-stage metamorphic-HEMT circuit with 50-nm gate length
- Design specifications
  - Passband frequency range 2-4 GHz
  - Input- & Output return loss ≥ 10 dB
  - Gain ≥ 30 dB
- On-chip DC-bias pads allow for individual Vd and Vg

Fraunhofer IAF

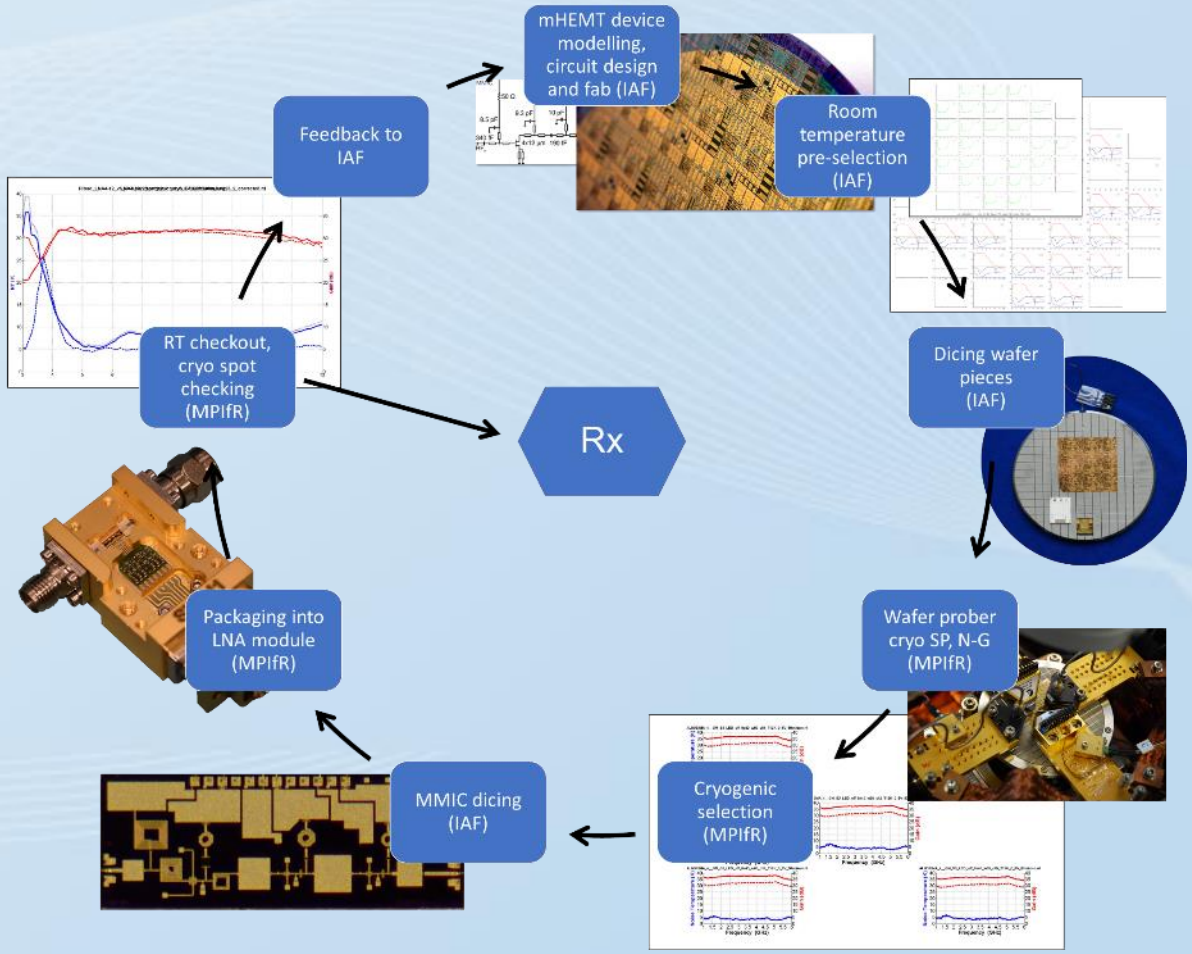
Kryo-mHEMT

DC bias considerations

- Large cryogenic FE mandates reduction of bias wires and voltage supplies
  - Shift from philosophy of having full external control of all individual MMIC supply voltages
  - Investigate influence of bias conditions on MMIC performance
  - Establish min. amount of preset gate voltages Vg required without affecting performance
- Two DC bias concepts studied
  - gate bus: 15 pins (2x Vd, 10x preset Vg, + 3 GND) with bondwire voltage line select per transistor
  - single gate supply line: 5 pins (2x Vd, 1x Vg_supply, + 2 GND) configurable voltage divider on PCB
- Cold FE PCB
  - Prototype V1 uses gate bus
  - Prototypes V2 will employ single Vg supply line
    - Maximum reduction in cryostat wiring and decreased DC connector footprint

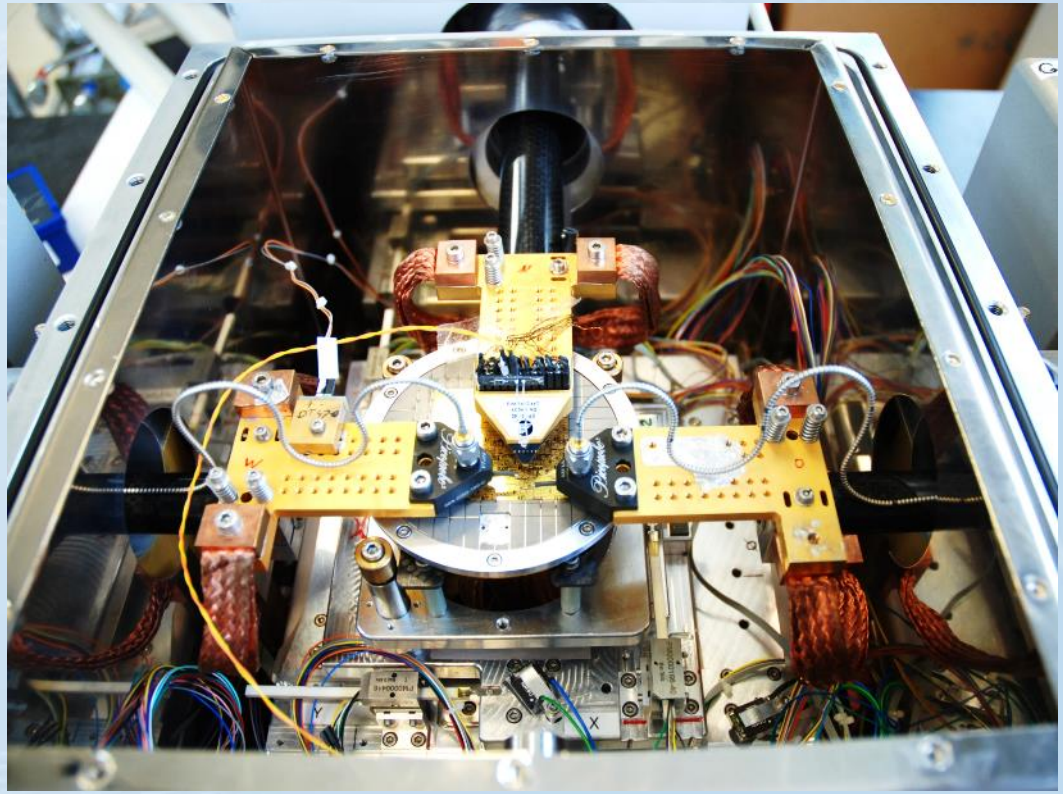
LNA development MPIfR <-> IAF

- @ IAF: device and circuit modelling, device fabrication, room temperature on-wafer testing, device pre-selection, closes optimisation loop to improve cryogenic device models
- @ MPIfR: cryogenic testing (on-wafer and package), package development and implementation, radio astronomy receiver applications



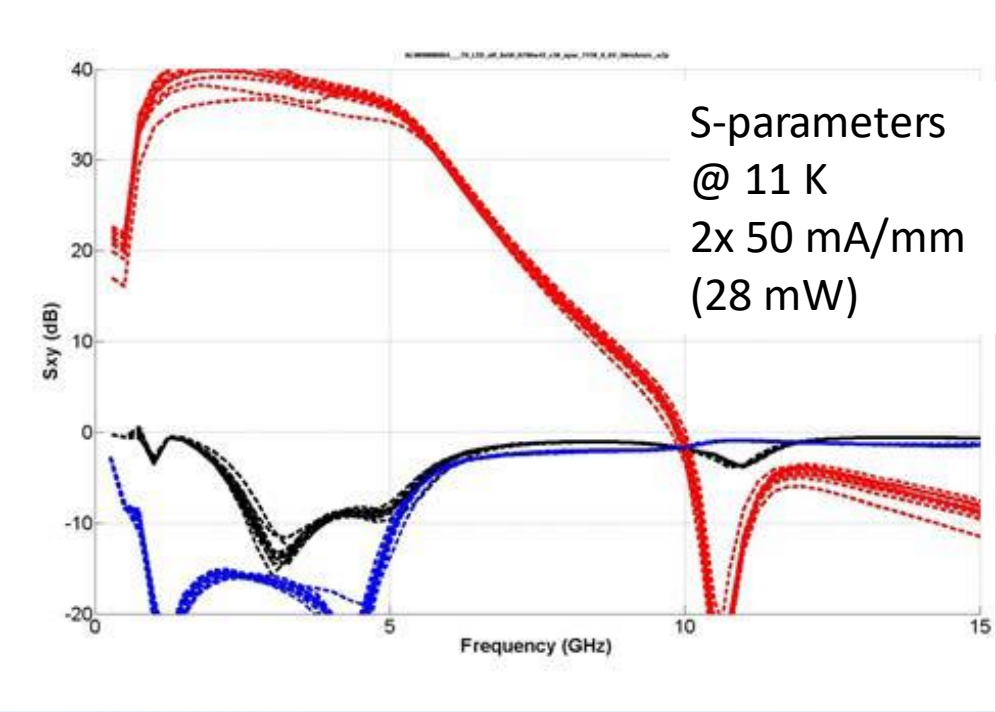
Cryogenic probe station

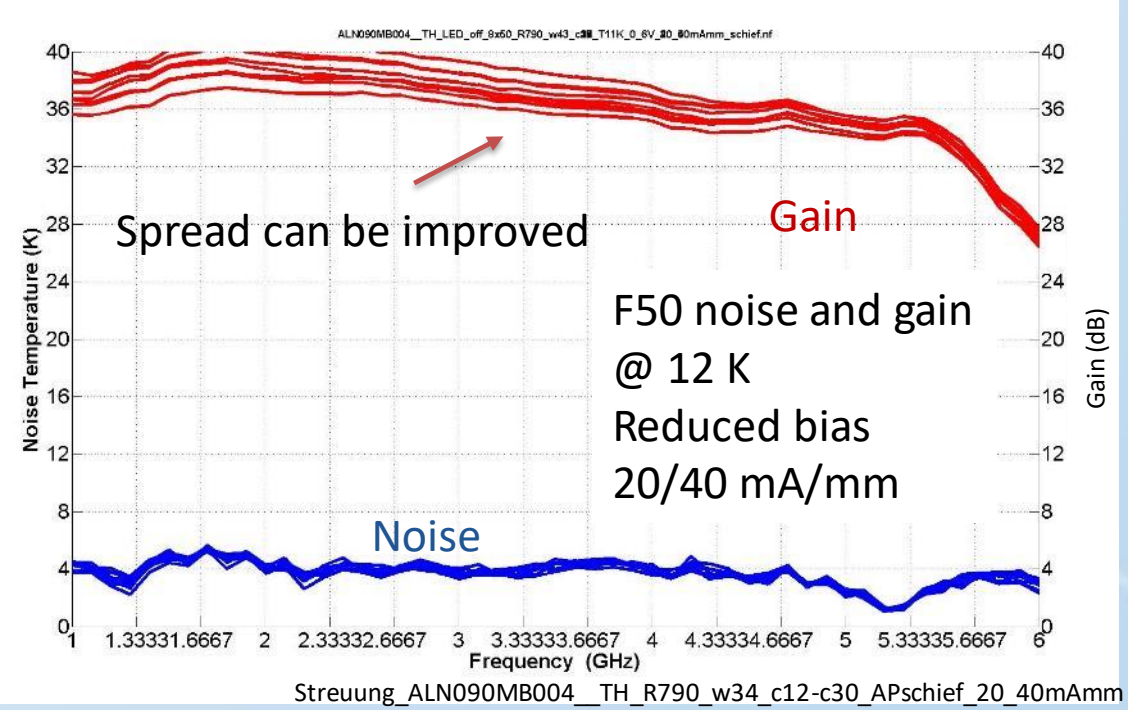
cryoPAF



In-house developed cryogenic probe facilitates selection of MMIC for larger volume LNA production

RF performance of CryoPAF MMIC (V1)





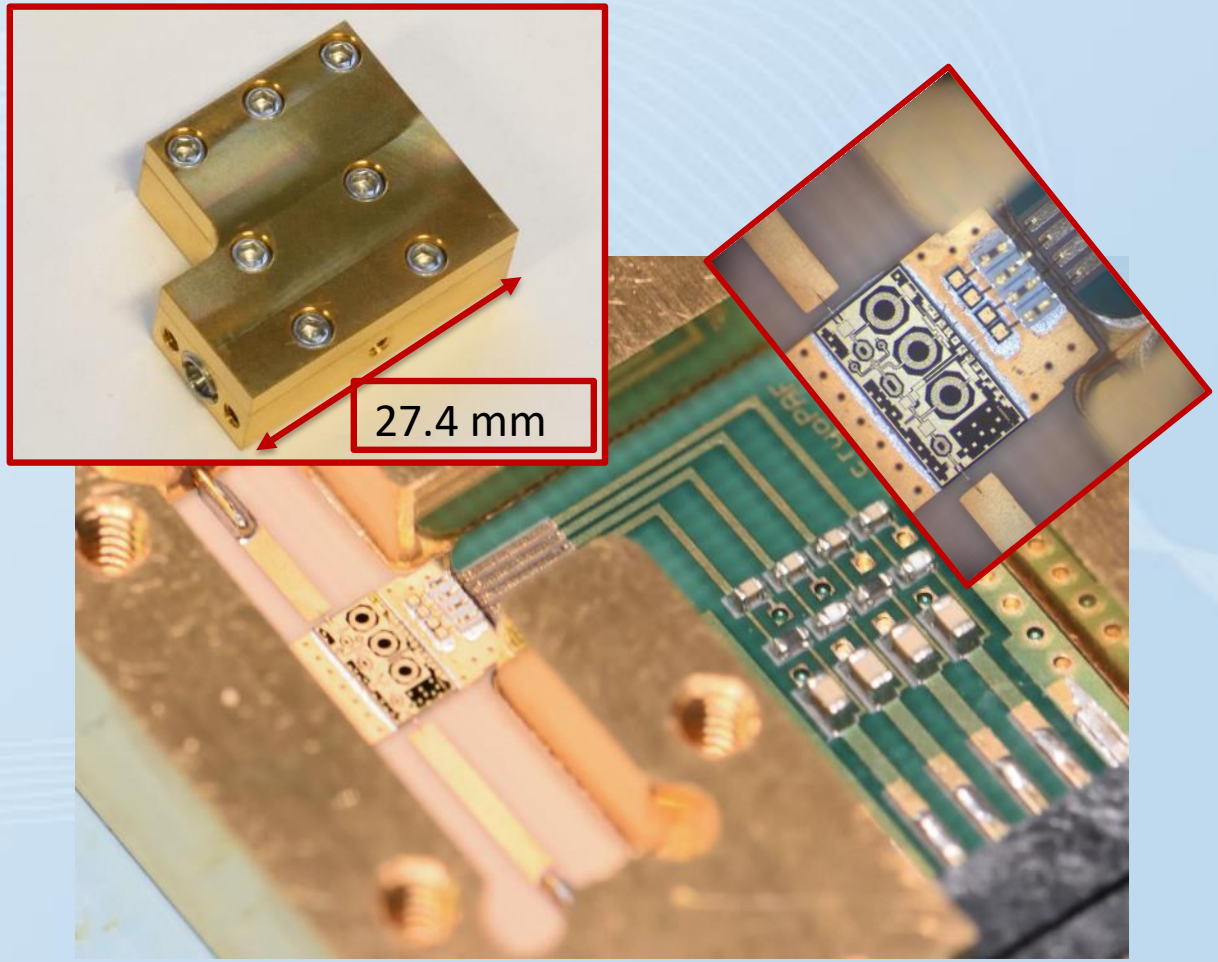
Streuung_ALN090MB004__TH_R790_w34_c12-c30_APschief_20_40mAmm

- first batch of MMIC V1 measured with **cryogenic probe station**
- single drain voltage $Vd_{1,2}$ = 0.6 V low noise operation established for both transistor stages and for all MMIC
- S param and F50 noise/gain vs. current densities for both transistor stages investigated
  - 20, 40, 50 mA/mm (also asymmetric) – low dissipation operation
  - Little performance trade-off for low power dissipation (current density) operation observed

Technology demonstrator for pad vias

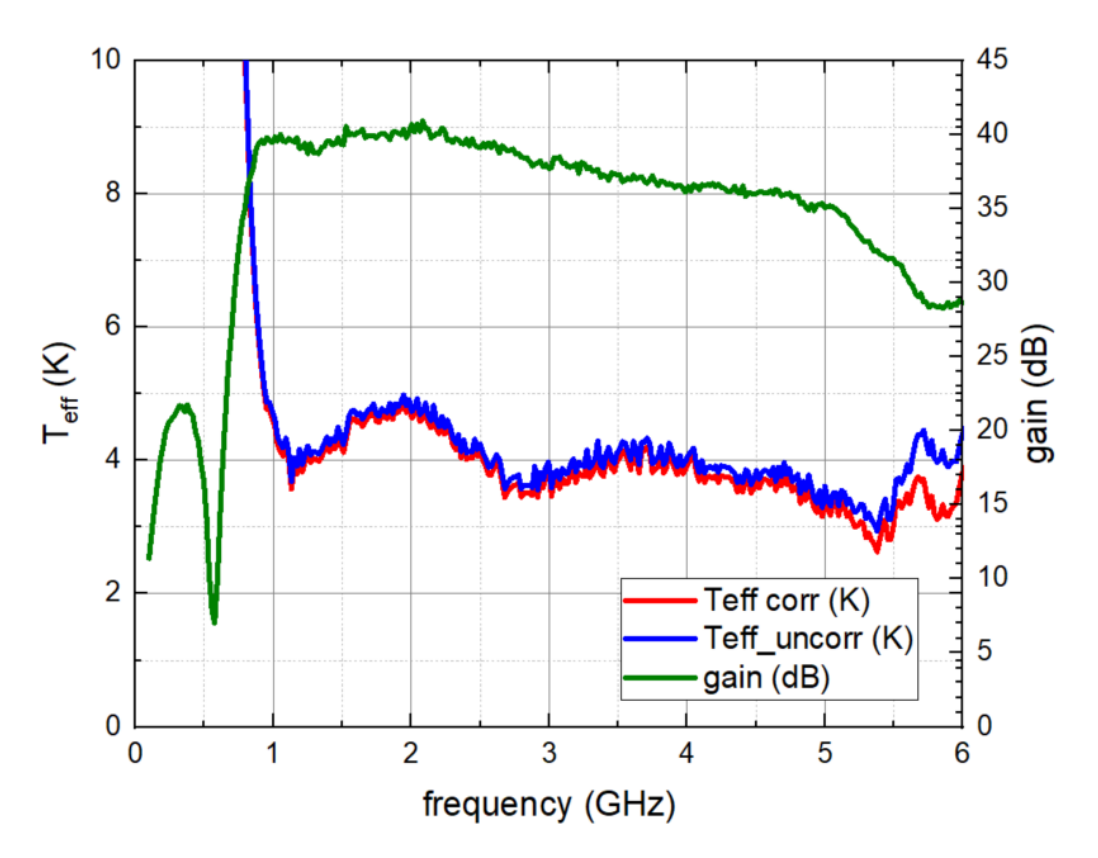
cryoPAF

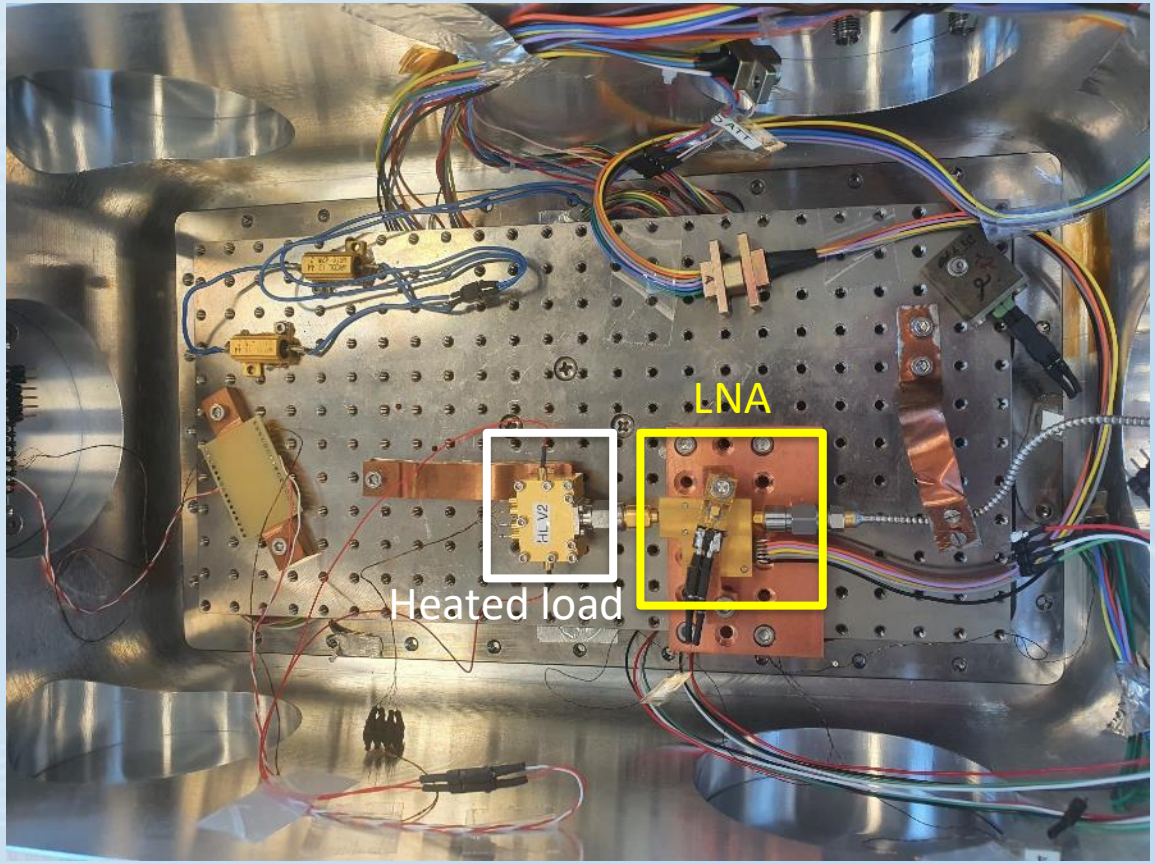
- Purpose: verify novel grounding scheme for MMIC
  - 10 mil MT77 with 0.15 mm diameter PTH pad vias
- LNA module used for evaluation of PCB technology
  - “conventional” with metal housing
  - established environment
- Also used for automated assembly tests at industry partner
- RF performance and cryo-mechanical
  - Compare to probed MMIC die



Technology demonstator for pad vias

cryoPAF

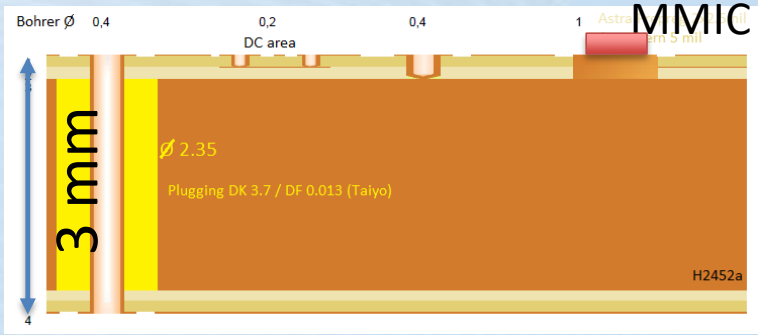


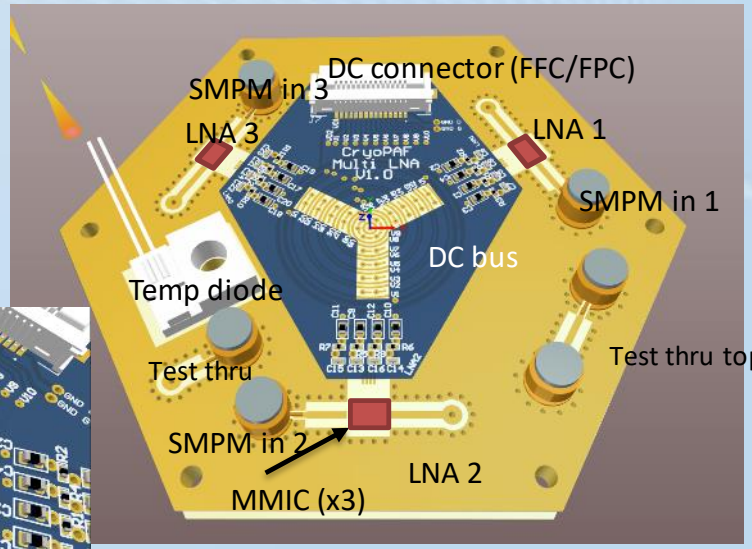


Performance similar to standard packaged LNA
and MMIC wafer prober measurements, ongoing evaluation

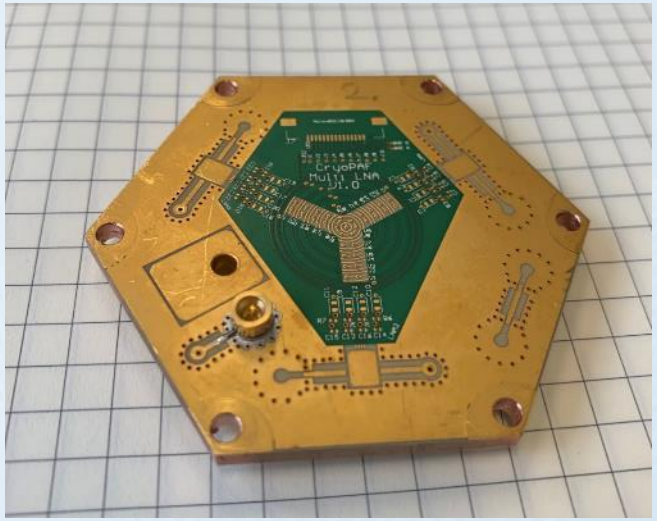
Technology demonstrator: planar assembly

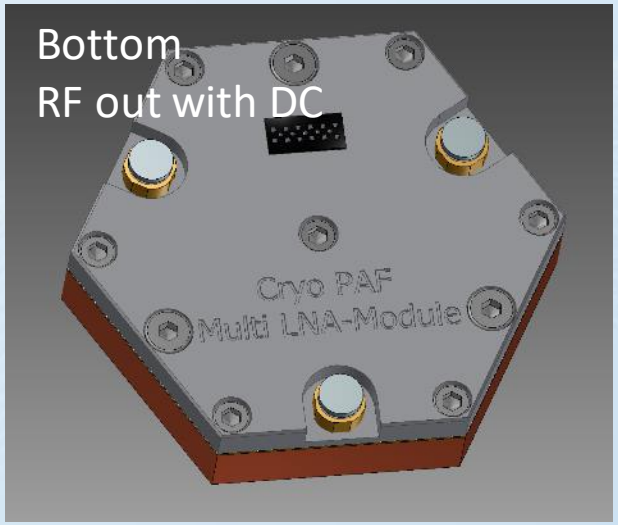
- Purpose: concept study for planar (tile) integration of PAF cold FE
- common multilayer PCB with several LNAs and “bias bus”
- Cu core PCB (3 mm) with profiled surface
  - Provides support, grounding, MMIC cooling
  - coax vias route RF signal from top to bottom
- cryo-mechanical evaluation of PCB successful
- Initial RF characterisation of coax vias p
- RF performance test deferred to later ti
  - Technology is of interest

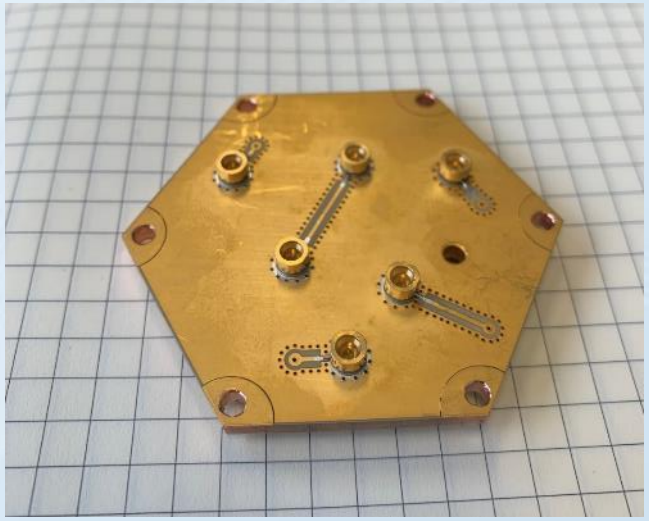


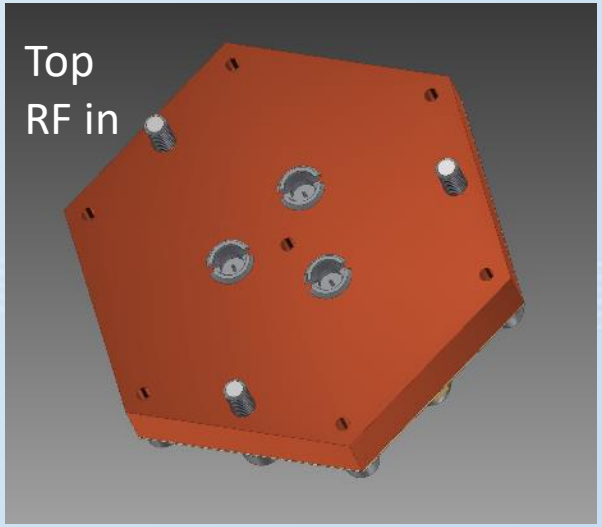


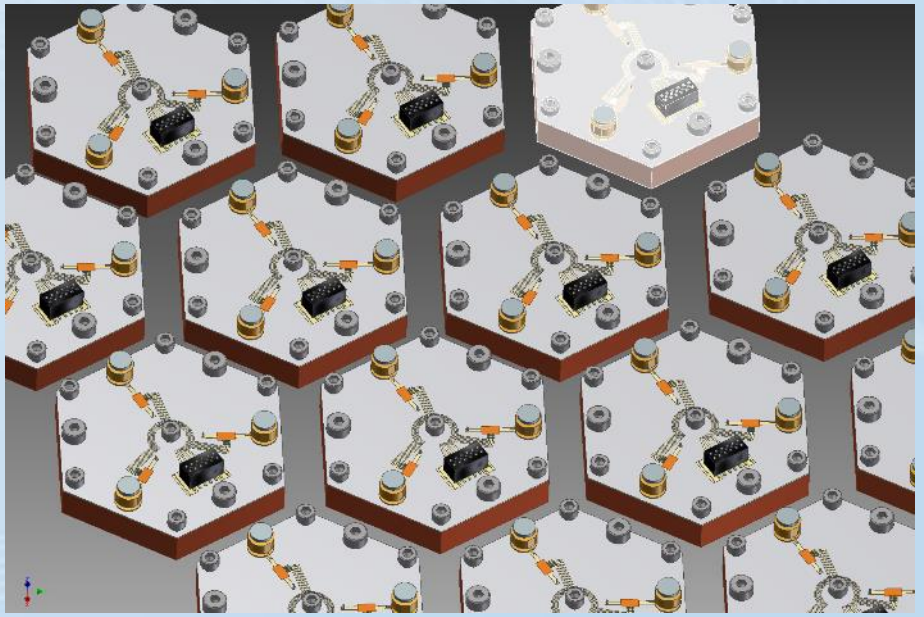
Technology demonstrator: planar assembly







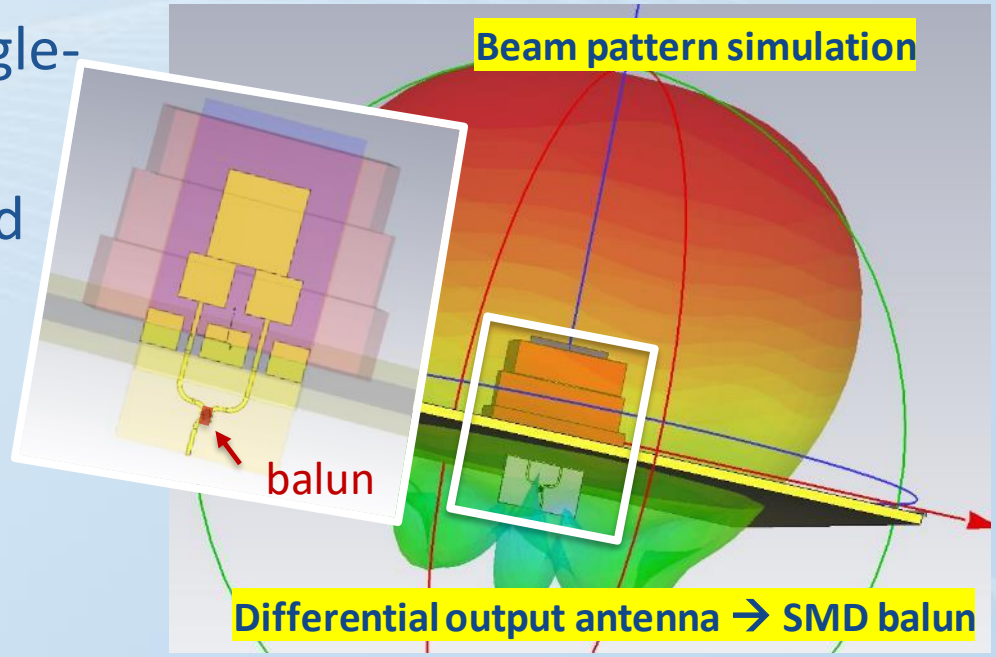


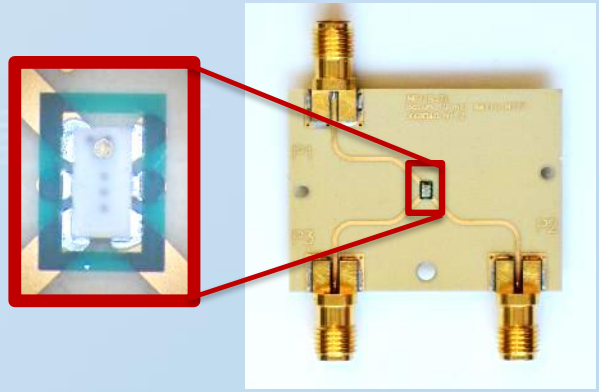


SMD balun cryogenic characterisation

cryoPAF

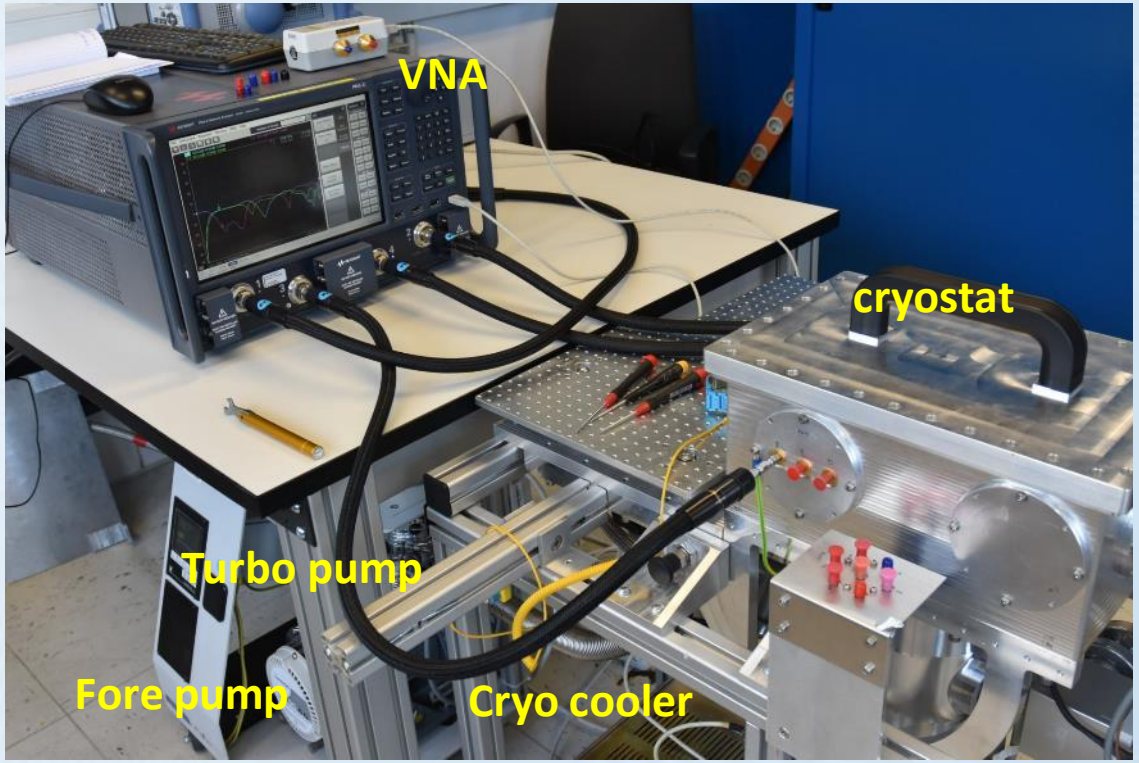
- Loop antenna requires balun circuit to feed single-ended LNA
- Commercially available SMD baluns investigated for cryogenic performance
- Advantages over planar circuit balun
  - Significantly more compact using 0603 footprint
  - Performance
- Connectorized evaluation boards designed
- BD2635 (TTM/Anaren) presented

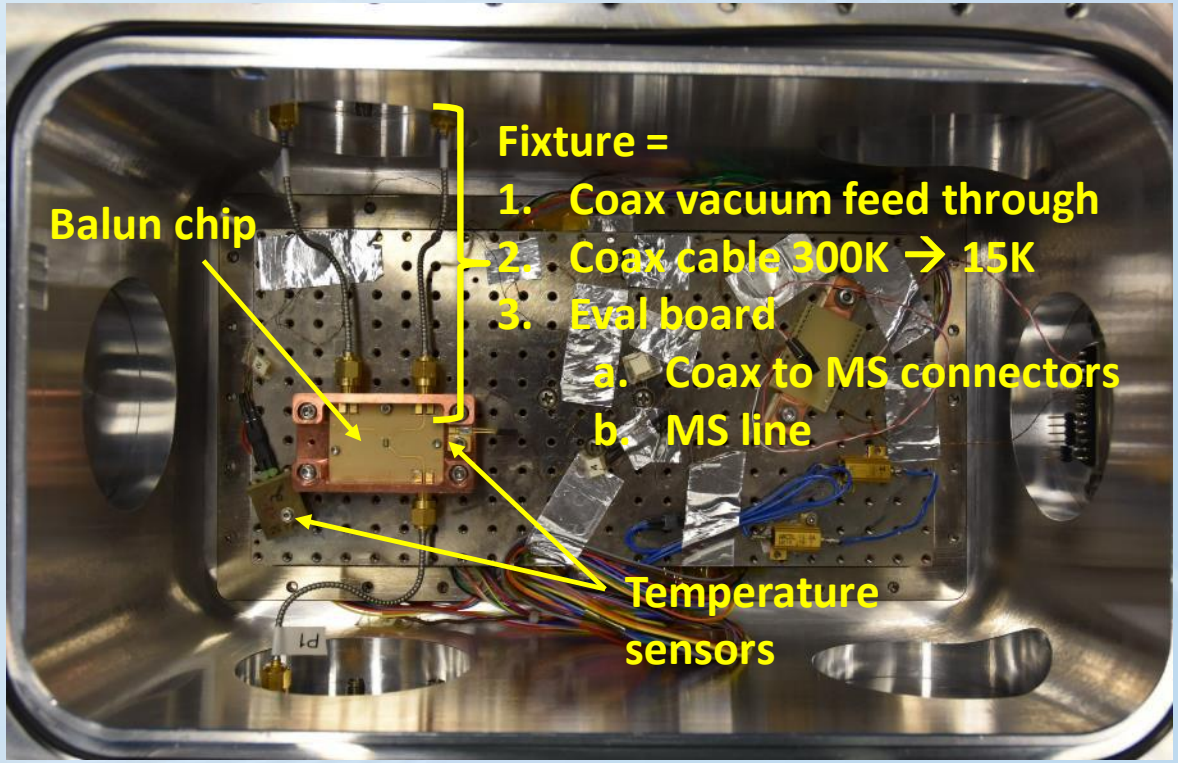




0603
1.69 mm x 0.94 mm

Cryogenic S-param measurement setup



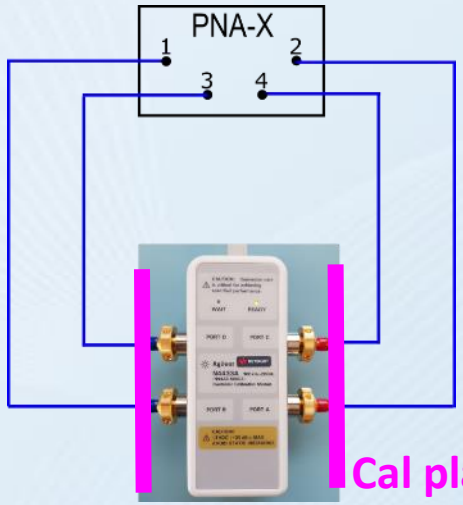


→ How to de-embed SP of balun chip without using multiple standards/cooldowns?

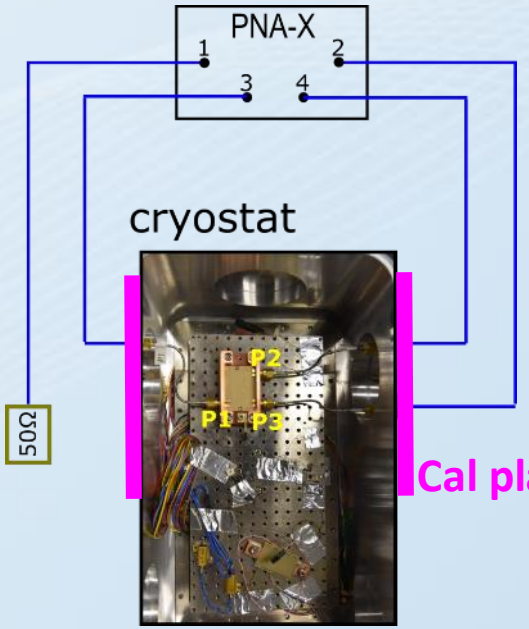
Solution: AFR (Keysight feature on PNA-X)

cryoPAF

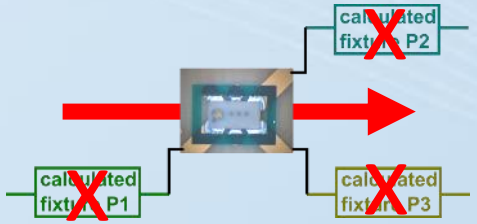
Step 1
Calibration of VNA cables



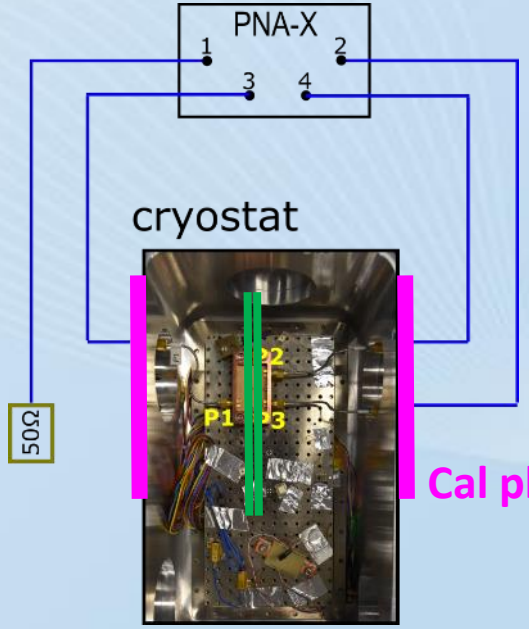
Step 2
Short Std meas @ cryoT



Step 3
AFR correction



Step 4
Balun meas @ cryoT



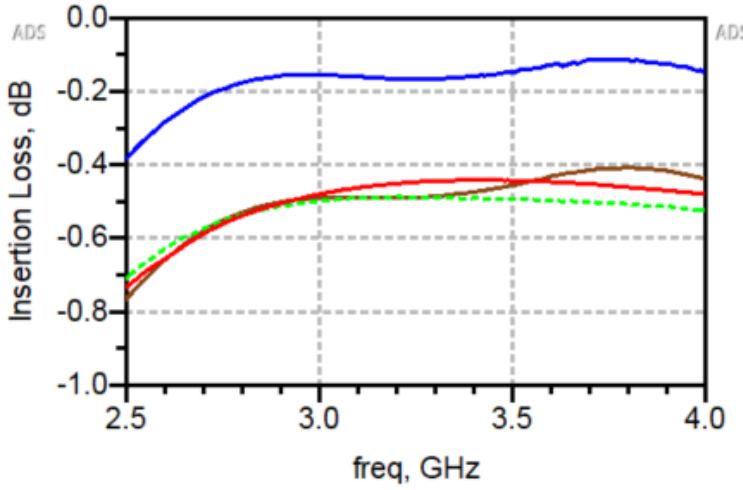
AFR = Single standard calibration procedure using TD to remove influence from fixture

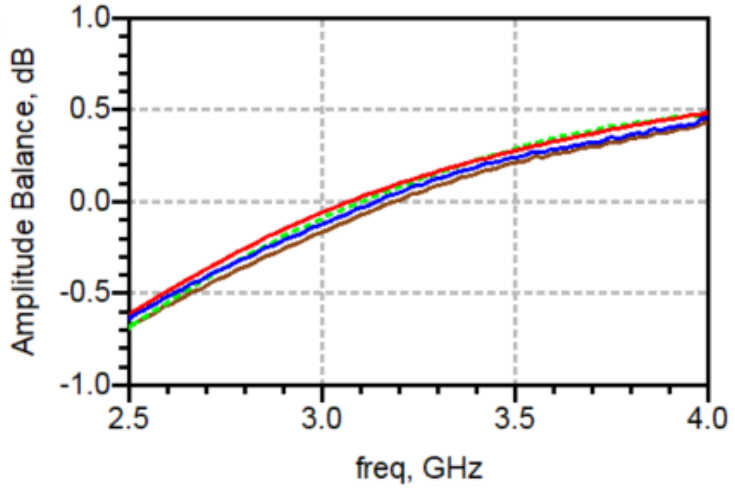
AFR correction plane

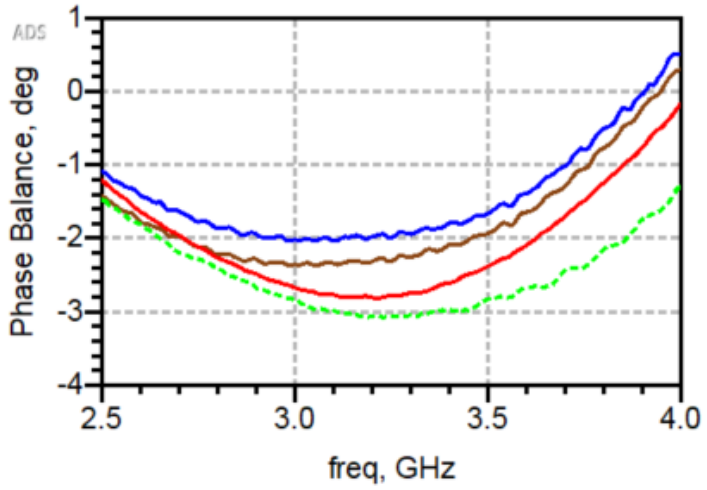
→ Only 1 additional cool-down required

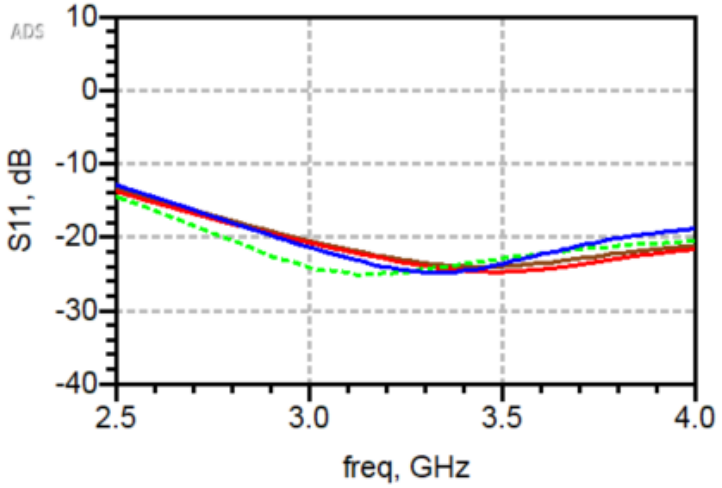
De-embedded (AFR) performance of BD2635

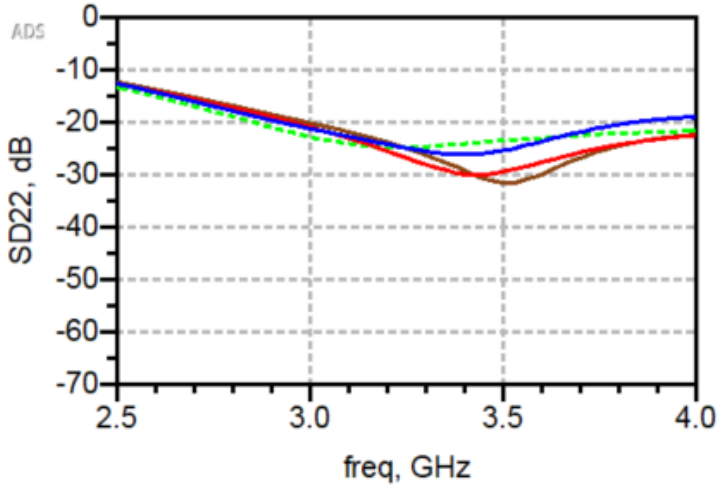
cryoPAF











AFR @RT outside cryostat
AFR @RT inside cryostat
AFR @cryoT
Anaren datasheet

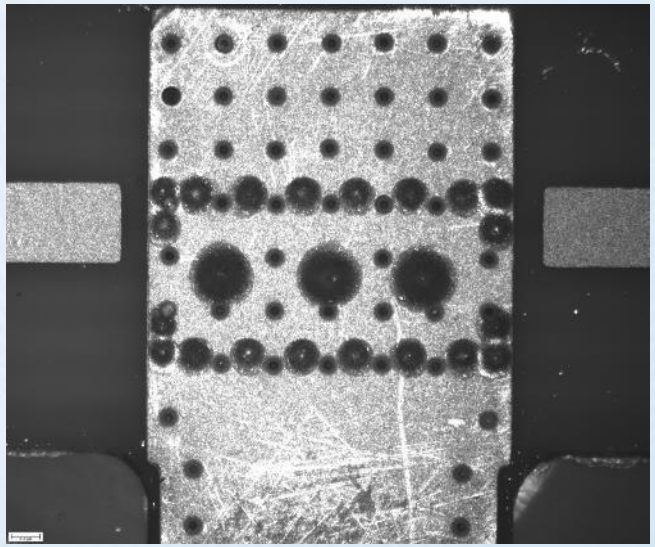
Loss < 0.2 dB @cryoT
RL > 15 dB
Δloss RT/cryoT ~ 0.3 dB

Measured at RT and 14 K

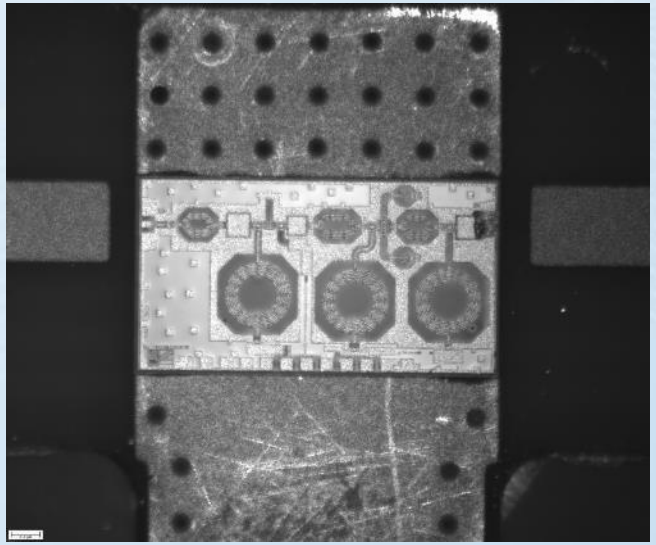
Electronic manufacturing

- LNA packages so far have been assembled by hand at MPIfR
- With CryoPAF cold FE module automated assembly of PCB components to be included into LNA production at MPIfR
- Evaluate most effective approach for cold FE PCB assembly
  - SMD components, MMIC, connectors, wire bonding
  - Hybrid approach contractor and MPIfR an option
  - Procurement of precision assembly tool -> all assembly in-house another option (favorable?)

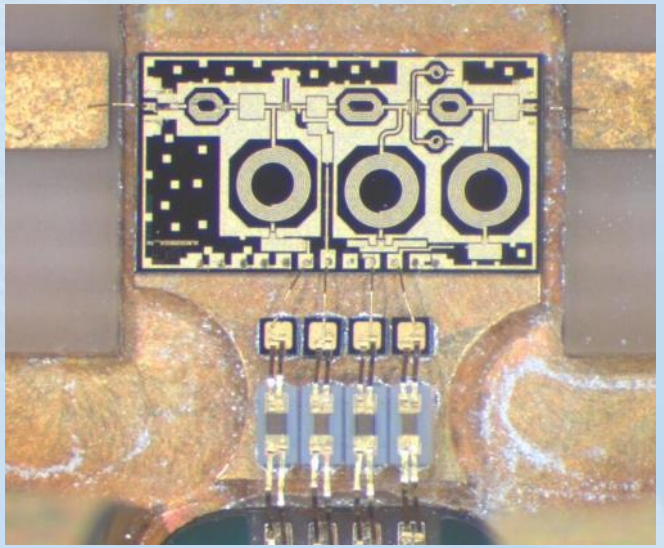
Automated placement of MMIC



Automated placement of conductive epoxy droplets (Epotek H20F)



Automated placement of MMIC



Automated placement of SMD and wirebonds

- Trials at industry contractor using technology demonstrator LNA package
  - excellent alignment capability (10 µm) shown for MMIC and SMD components
  - New trials to investigate MMIC handling using custom pick-up tool (mechanical and ESD)

Current work items and outlook

- RF optimisation
  - Verify cold FE prototype PCBs and sub-circuit sections
  - Verify pad via approach for MMIC (initial look positive)
- Cryo-Mechanical and thermal behaviour
  - Clamshell housing
  - Thermo-Mechanical interfacing PCB to housing, receiver structure and connectors
  - Cooling of MMIC in housing
- Electrical
  - alignment tolerances of electrical interface antenna plane
  - DC bias configuration (configurable voltage dividers for $Vg_{1,2}$ on PCB)
  - selection of connector I/O
- Establish best route for effective automated assembly
  - Safe handling of MMIC
- Ramp up to production
  - Freeze designs, procurement and start fabrication