pHEMT Characterisation and SSEC Extraction from 4 K to 290 K

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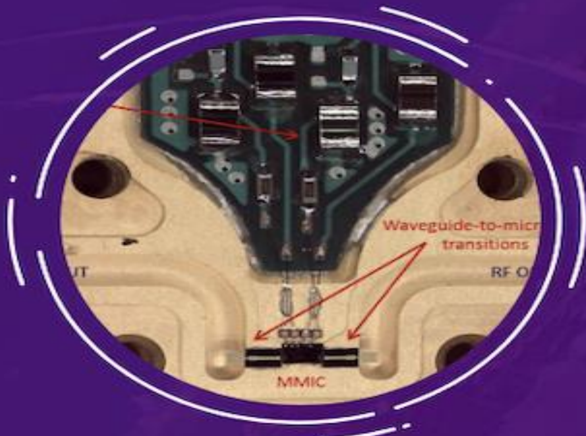
Group

University of Manchester

FACILITIES AND CAPABILITIES



Development of Microwave Components

Design of millimetre and sub-millimetre wavelength devices using MMIC technology.

S-parameters and Noise Measurements

Capability to measure S-parameters up to 330GHz and noise up to 110GHz

Integrated circuits and packaged devices

Measurements of MMICs and transistors to improve models and design

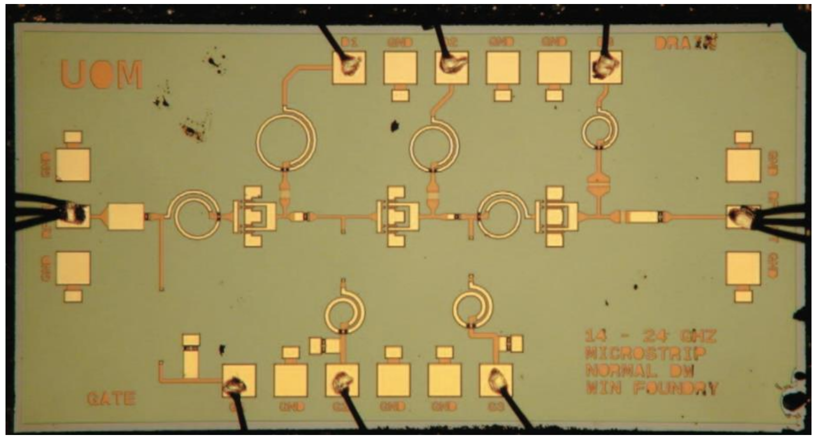
Cryogenic facilities

On-waffer cryogenic measurements at 4K and RF cryostat to meassure down to 300mK

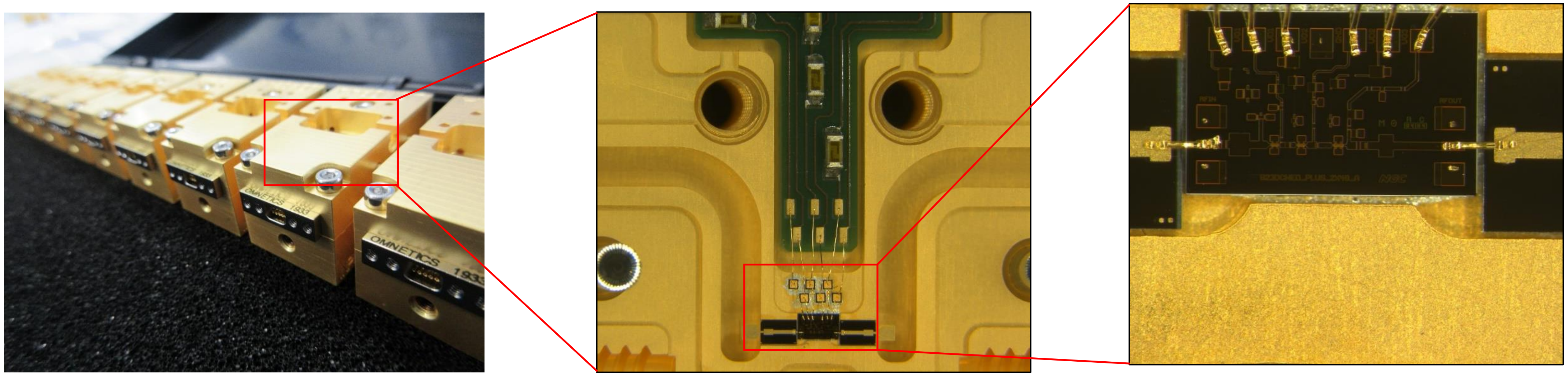
Focus on design and development of LNAs and front-end receiver instrumentation up to 400 GHz

MMIC LNAs Design in ARIG

MANCHESTER 1824
The University of Manchester



- 13.6 to 24 GHz LNA designed by Daniel White, William Mcgenn et. al
- WIN PP10-10 pHEMT technology
- Published in: [2019 IEEE Asia-Pacific Microwave Conference (APMC)]



- 75-110 GHz (ALMA Band 2 + 3) MMIC LNAs published by David Cuadrado-Calle, et. Al, 2017
- Three-stage MMICs using 35nm InP process at Northrop Grumman Corporation (NGC)

1. Challenges of MMIC LNA Design for PAF

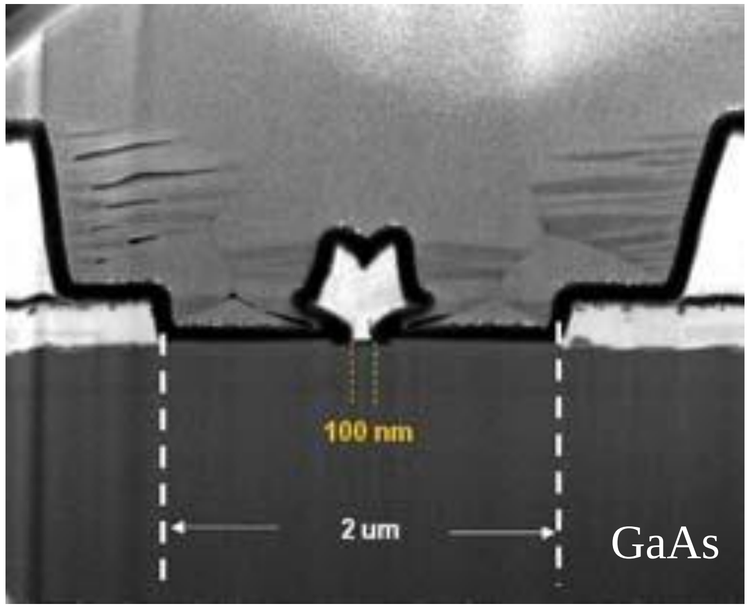
ALMA

ASKAP

- **A massive number of LNAs are required for Radio Telescope Arrays and Phase Array Feeds. These LNAs should have good consistent performance when there are used in a PAF.**
- **An accurate cryogenic model of transistors is needed for MMIC LNA design.**
- **Shortening the development cycle and reducing the price are also important considerations.**

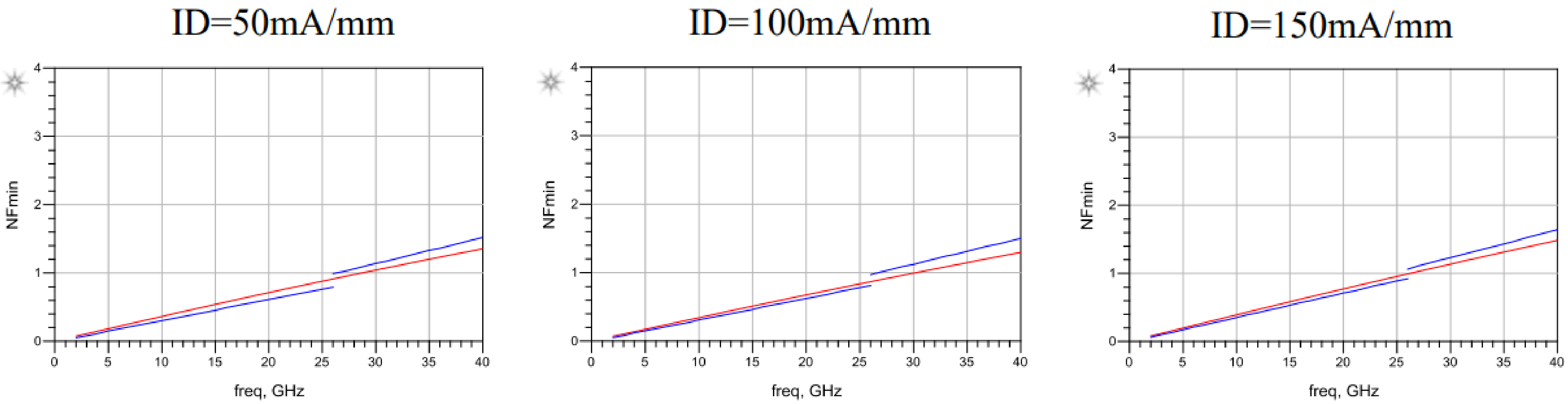
2. WIN and Diramics Commercial pHEMT Technology

1. WIN 0.1 um GaAs pHEMT technology



www.microwavejournal.com

- 100 nm gate length
- F_t greater than 135 GHz and F_{max} over 185 GHz
- The high degree of process maturity and commercially available technology
- Two 150mm GaAs fabs with monthly capacity of 24,000 wafers (2016)



Device 15D04A075

Vds = 2.0 V

Ids = 50mA /mm, 100mA/mm and 150mA/mm

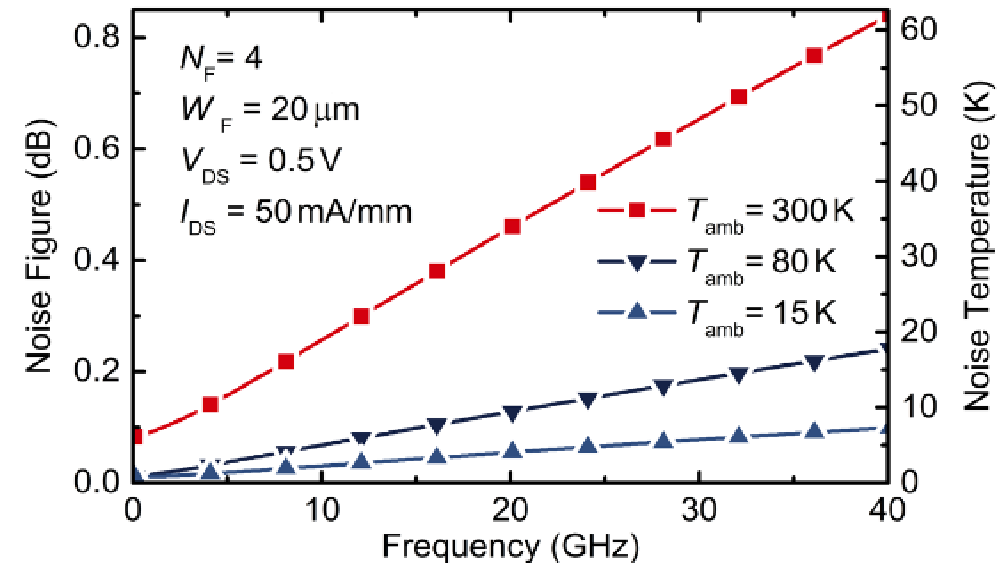
PP10-10 0.10um pHEMT Model Handbook_Ver1.3.3

2. Diramics PH-100 InP Technology

Available Dimensions for the pH-100 Technology	
Gate Length:	100 nm
Finger Width:	10 µm – 150 µm
Number of Fingers:	2 / 4 / 6

Basic Characteristics of a 4 x 20 µm Device (incl. bond-/probe- pads)

	300 K	15 K
f_T:	220 GHz	235 GHz
f_{MAX}:	550 GHz	800 GHz
gm:	1250 mS/mm	1500 mS/mm
NFmin (@30GHz)	0.6 dB	0.08 dB
Tmin (@30GHz)	43 K	5 K



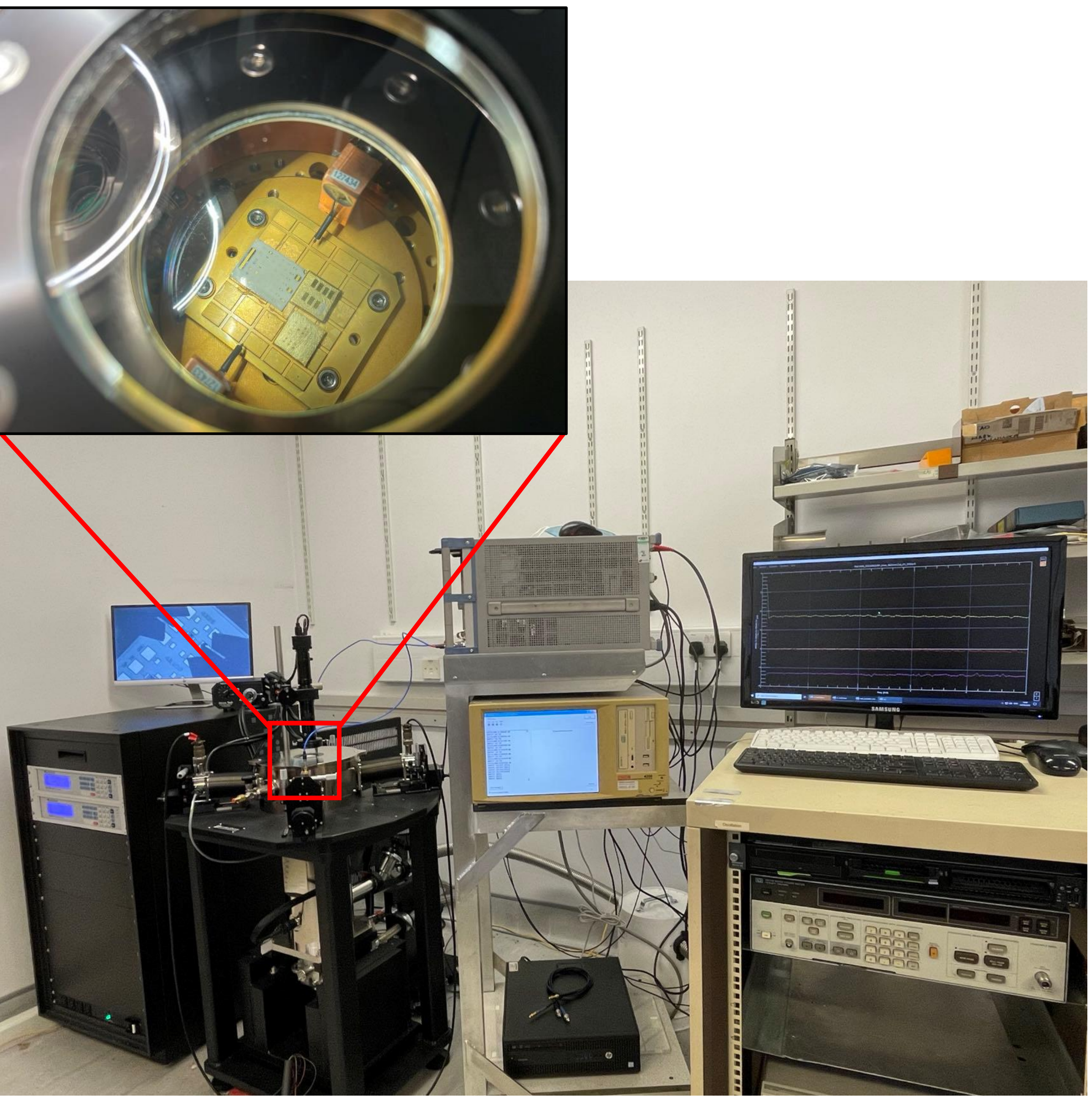
www.diramics.com

- 100 nm gate length InP-based pHEMT
- LNAs based on this technology are used in Yebes Astronomical Observatory and ESA ESTRACK
- MMIC process is possible

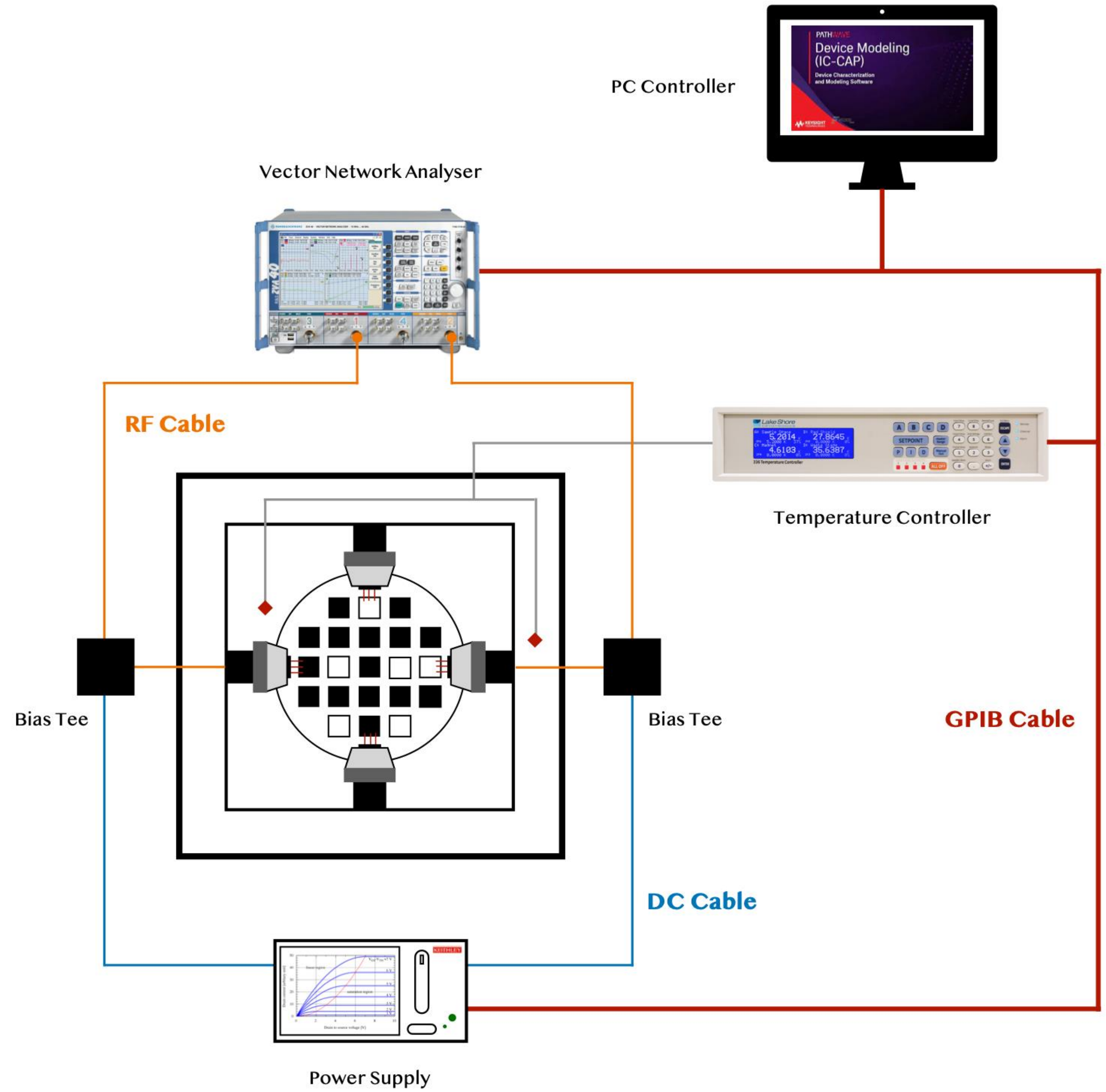
Low Noise Amplifier With 7-K Noise at 1.4 GHz and 25 ◦C. Sander Weinreb et. al 2021.

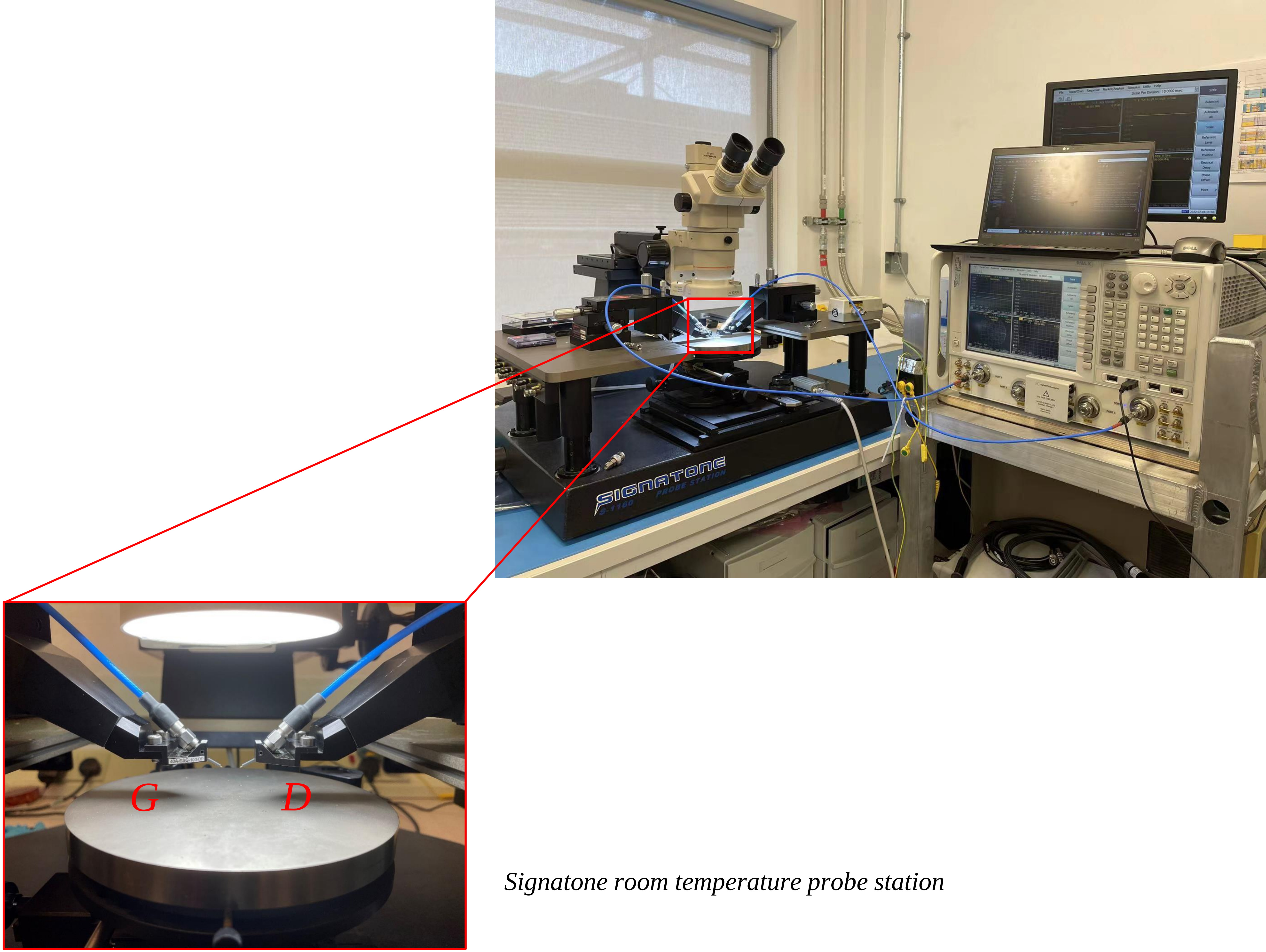
3. Transistors Characterizing and Modelling in ARIG

1. Probe Station Measurement System



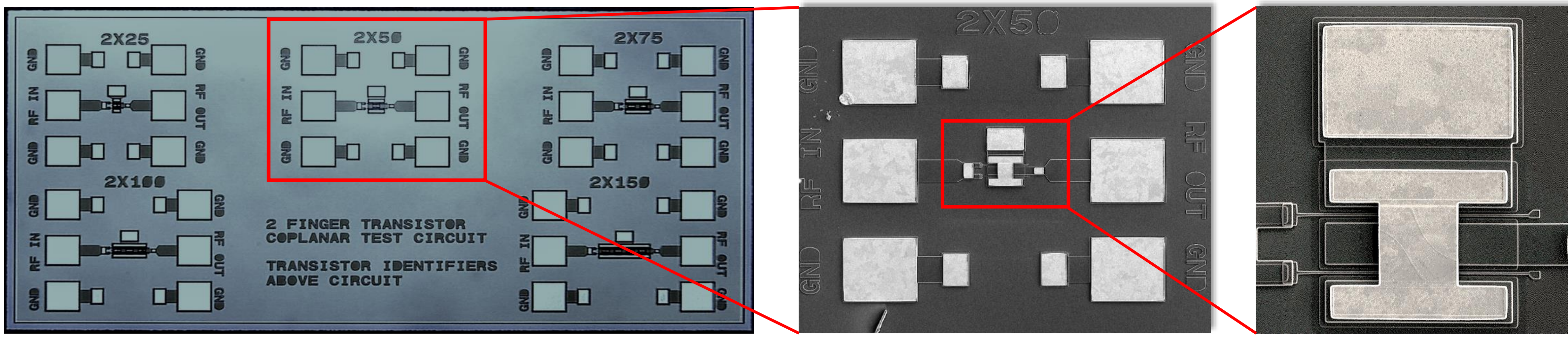
Lakeshore 4 K cryogenic probe station

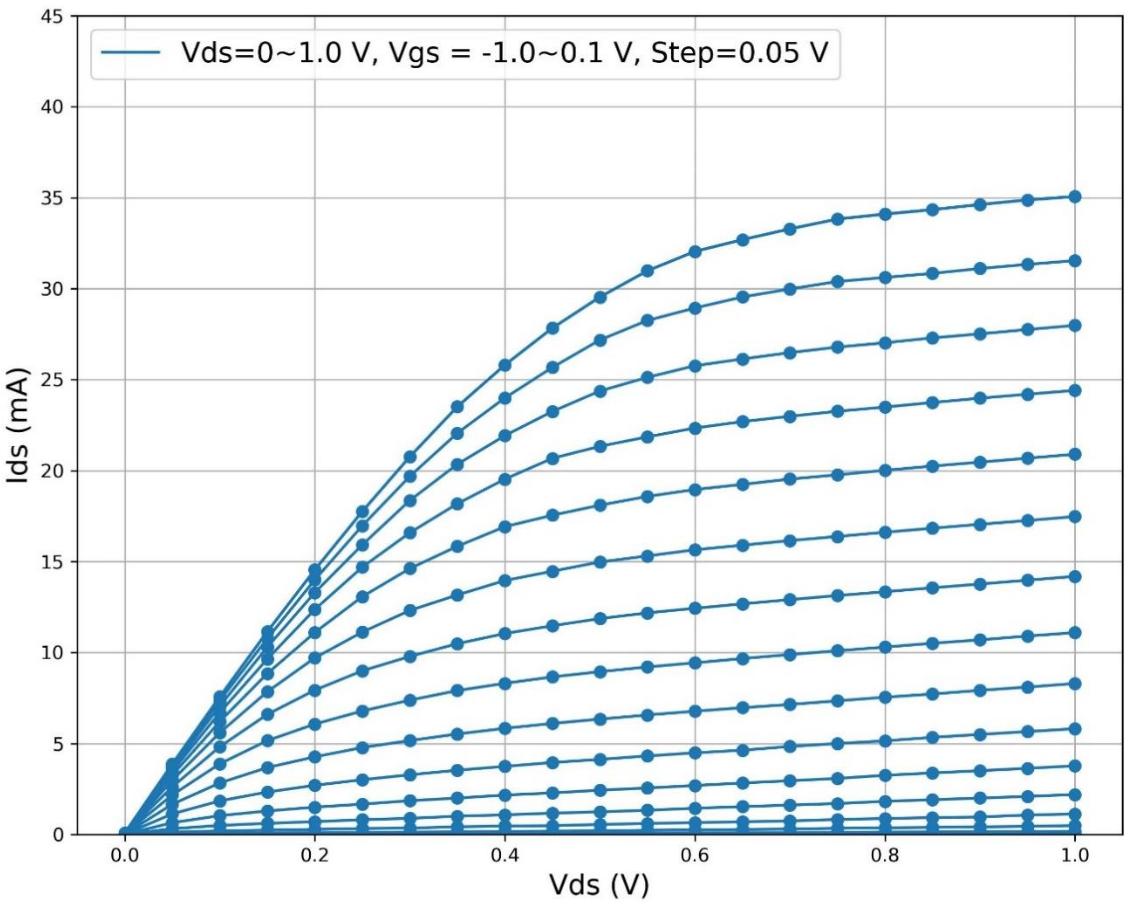




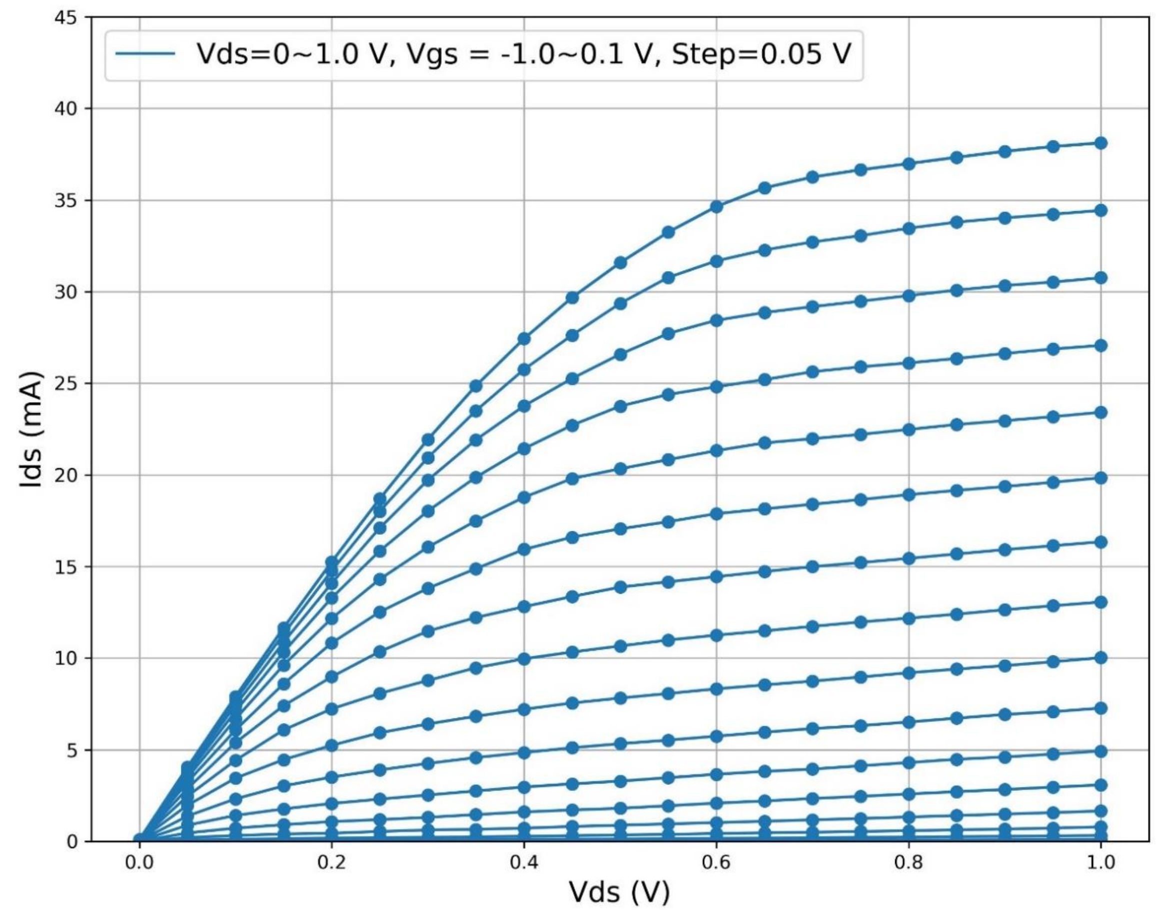
Signatone room temperature probe station

2. DC Measurement at 290K, 15K and 4K environment temperature

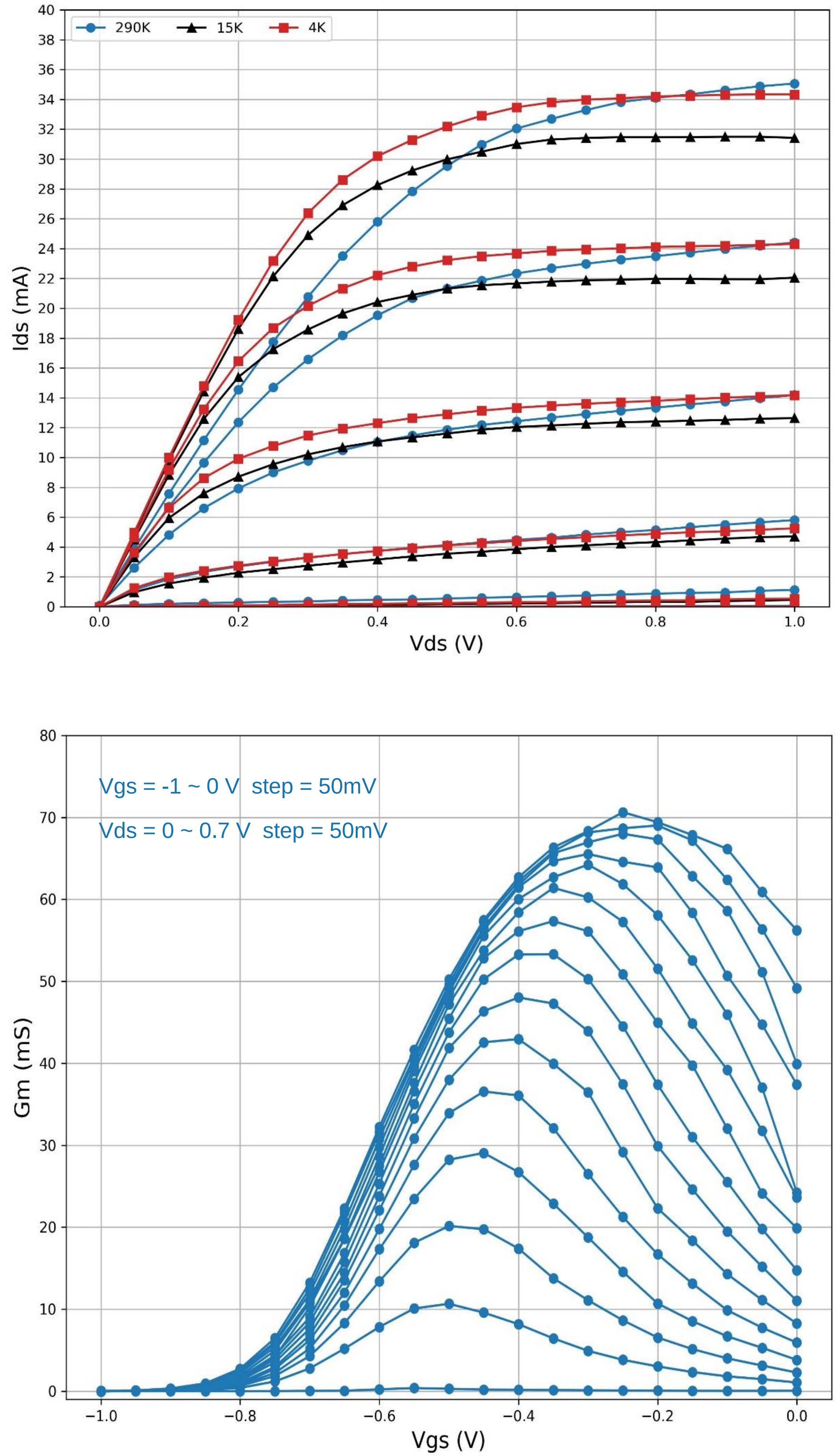




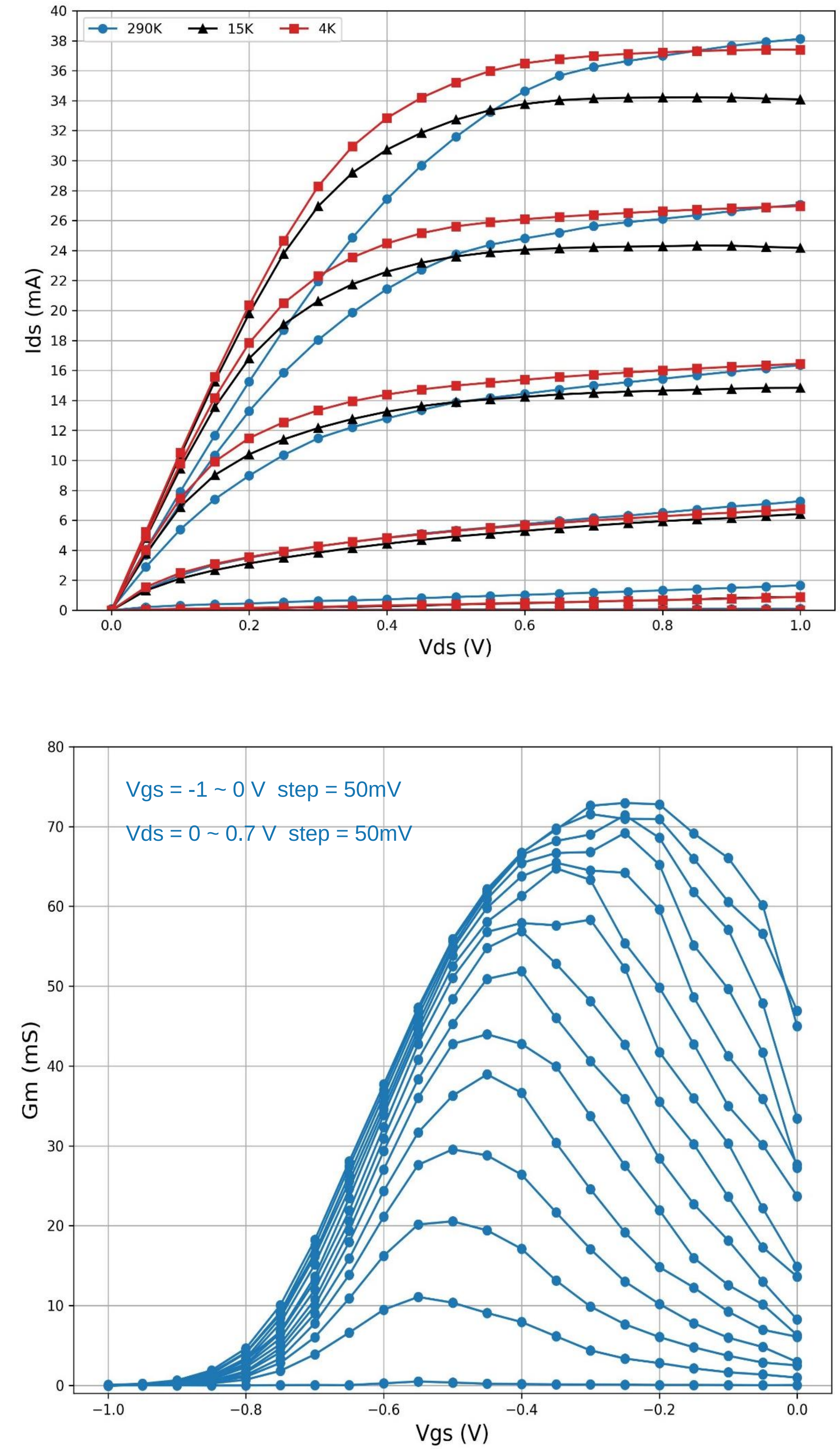
2F50um



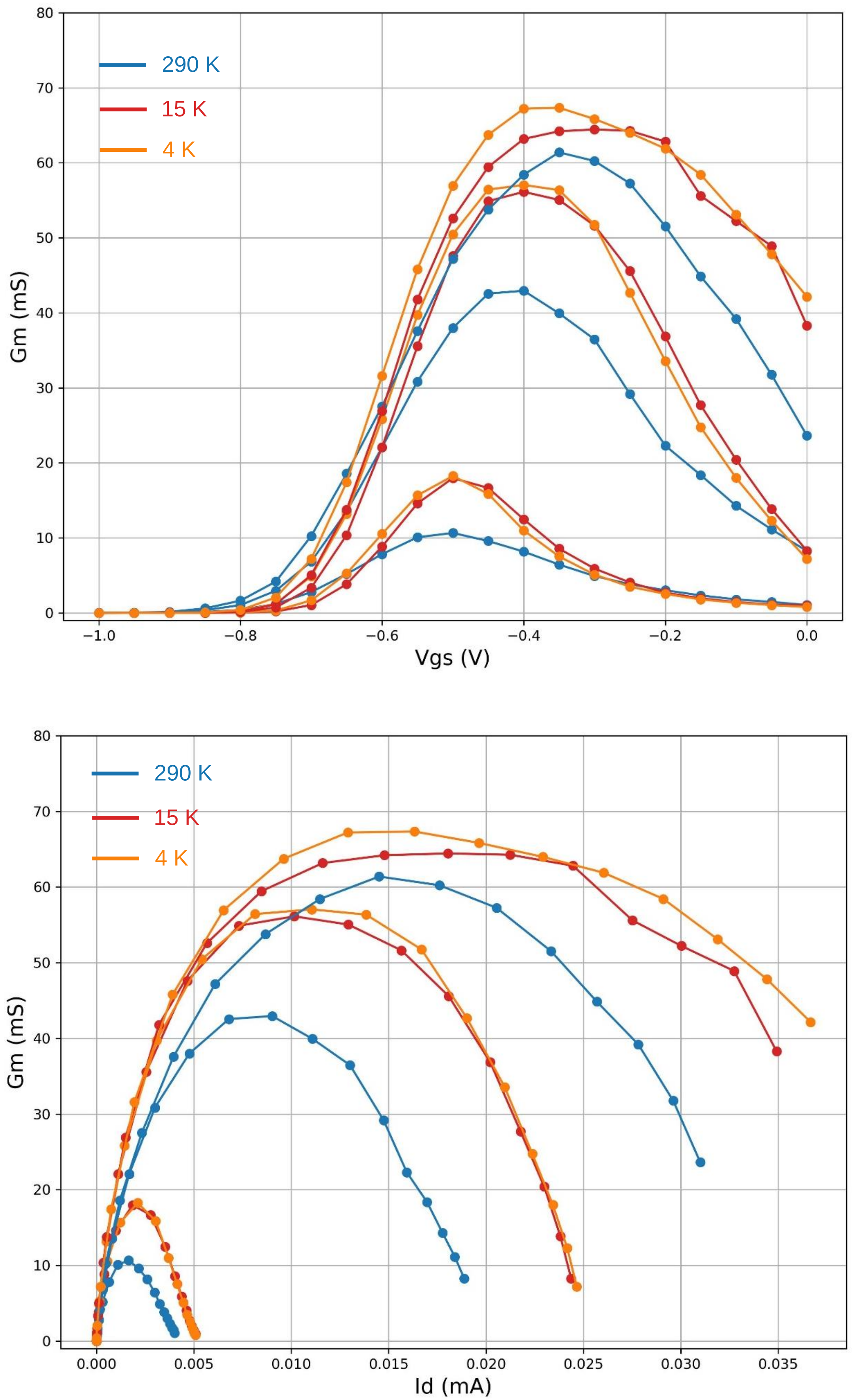
4F25um



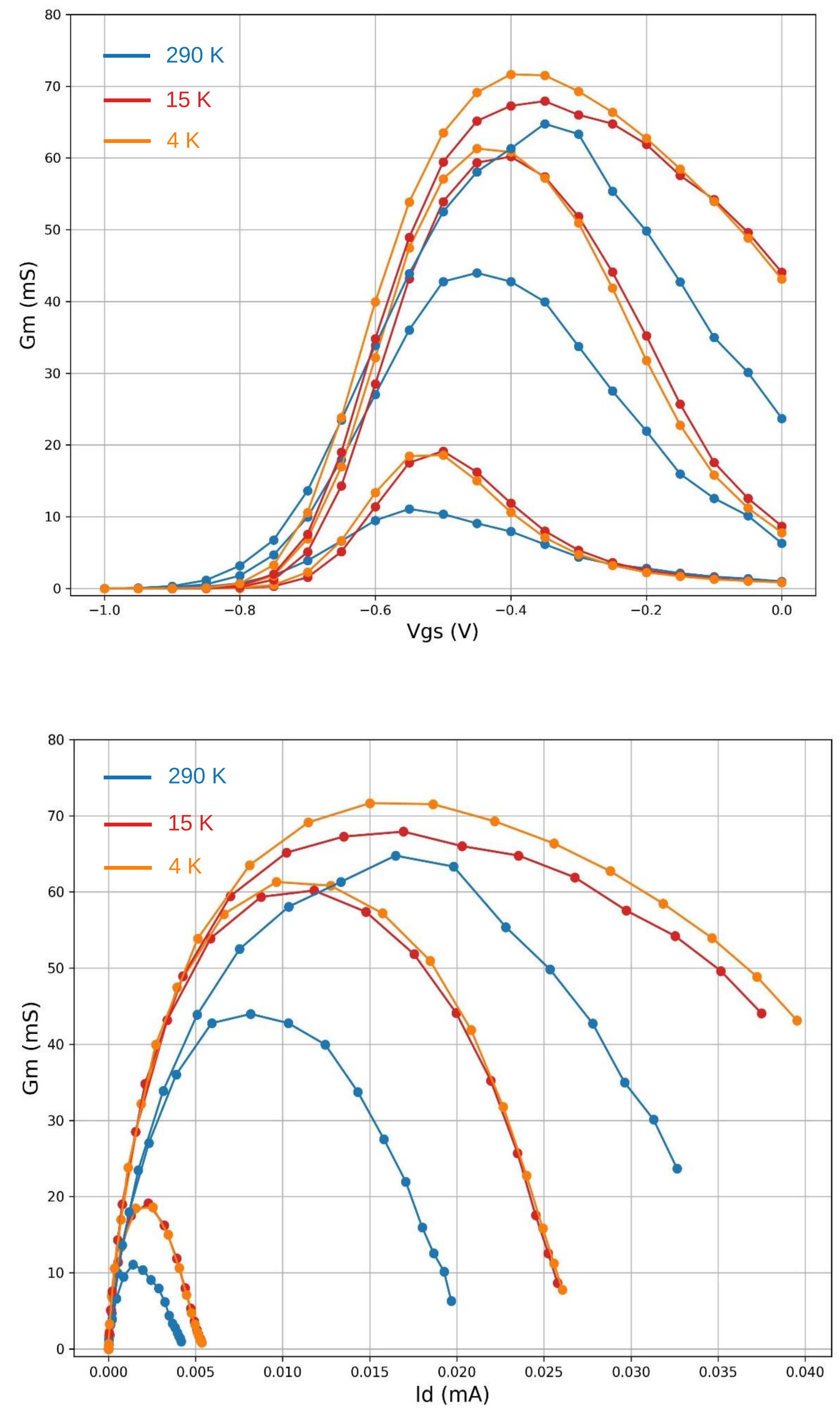
2F50um



4F25um



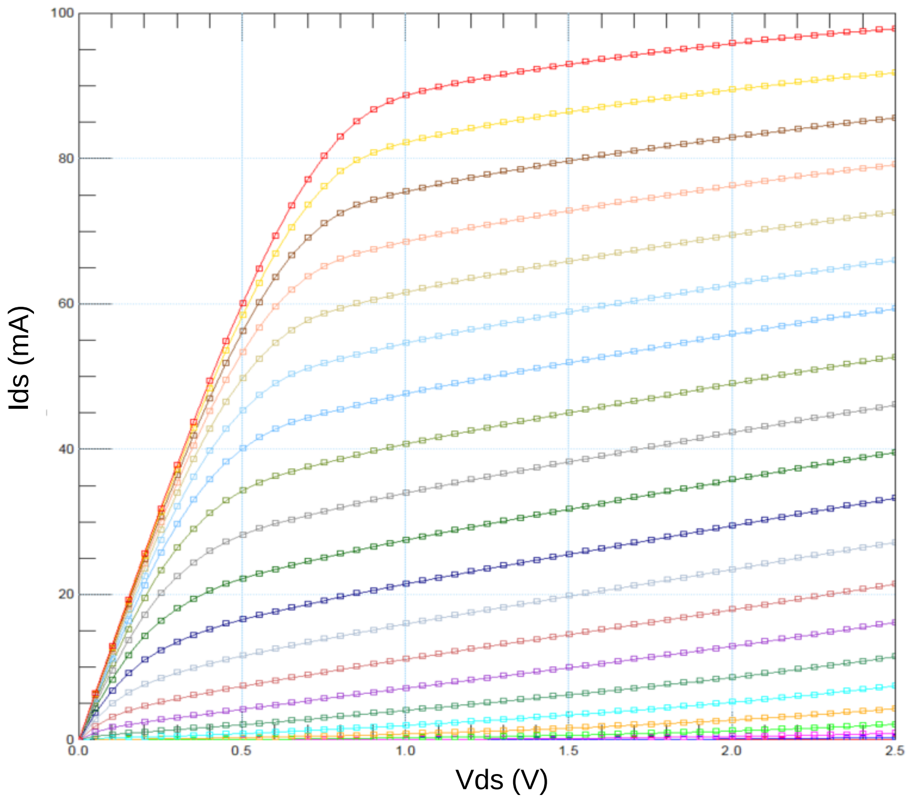
2F50um

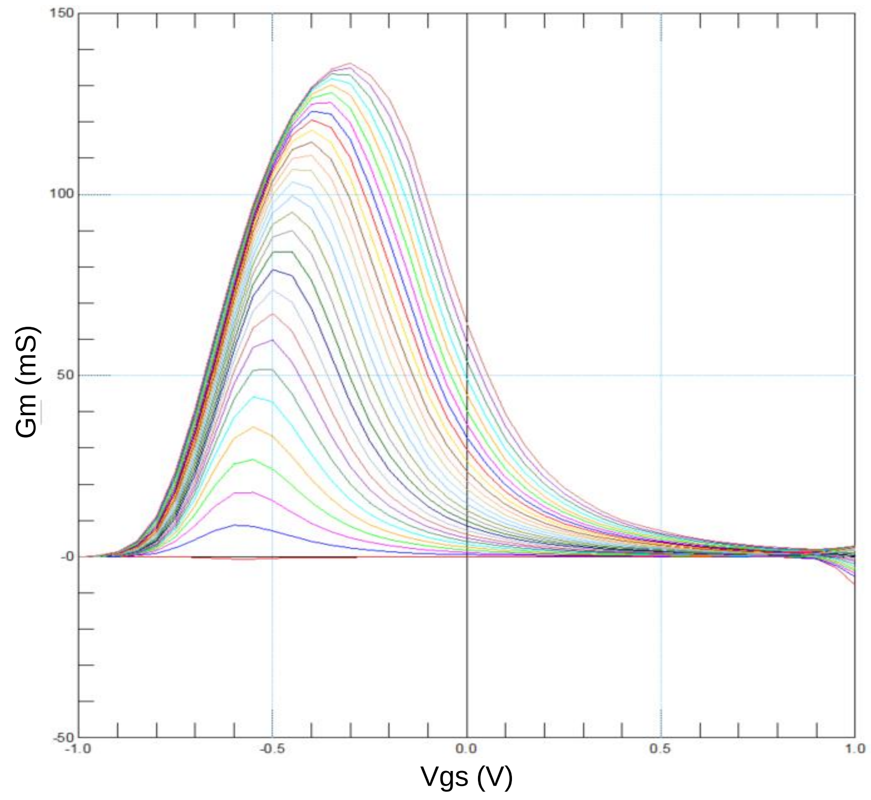


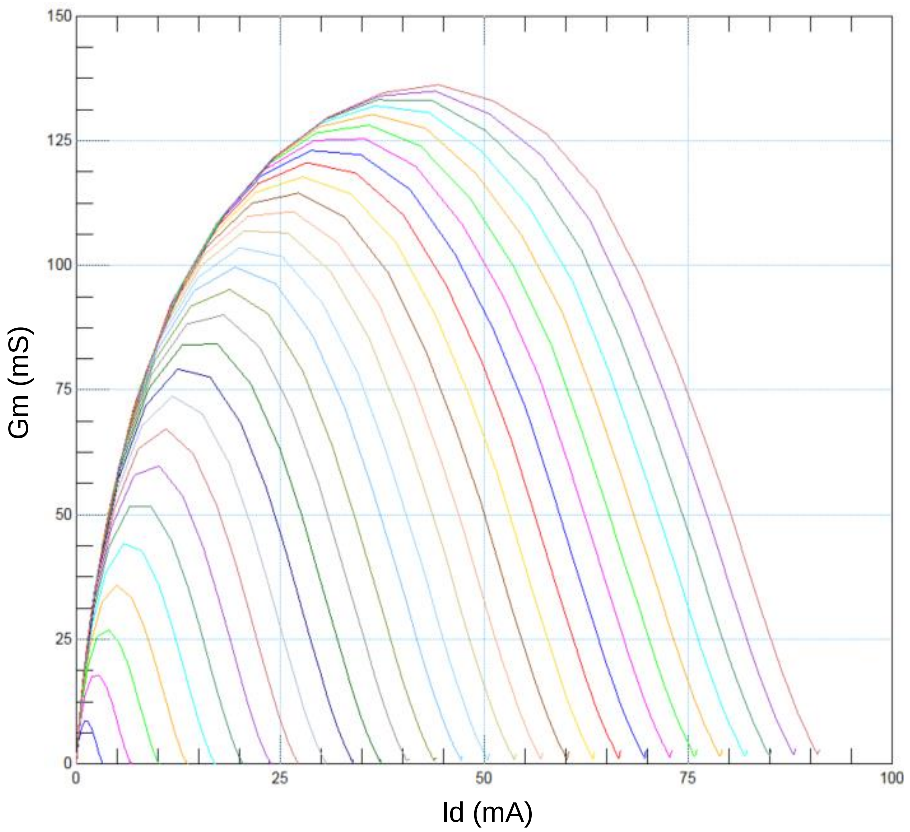
4F25um

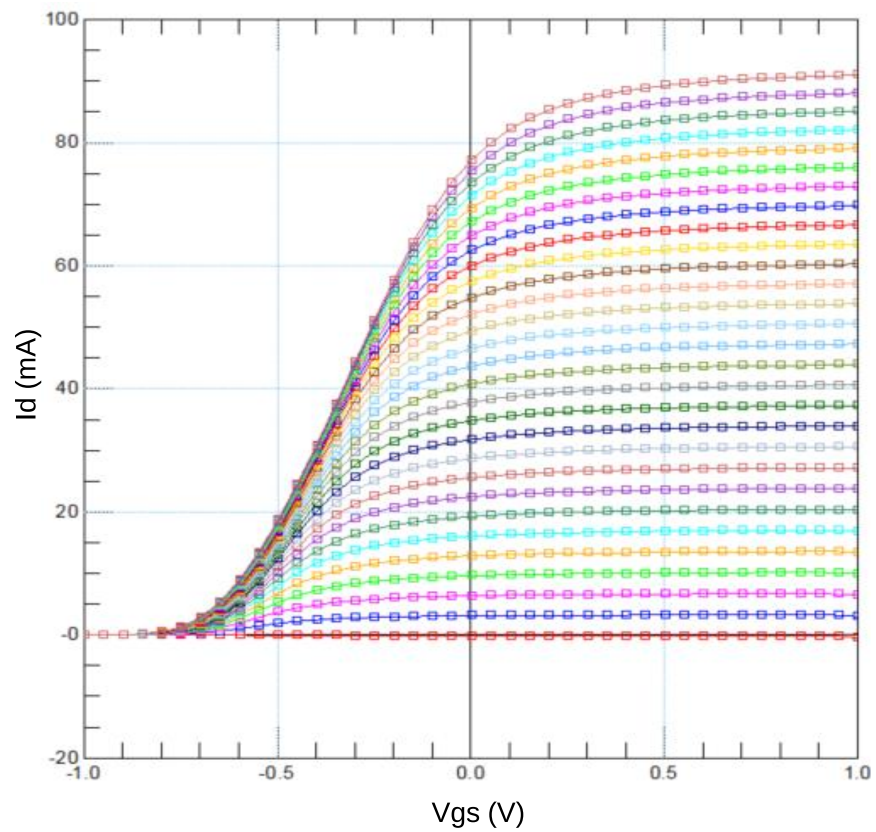
3. DC Measurement at 290 K and SSEC model extraction

➢ ***W4F50 um transistor***

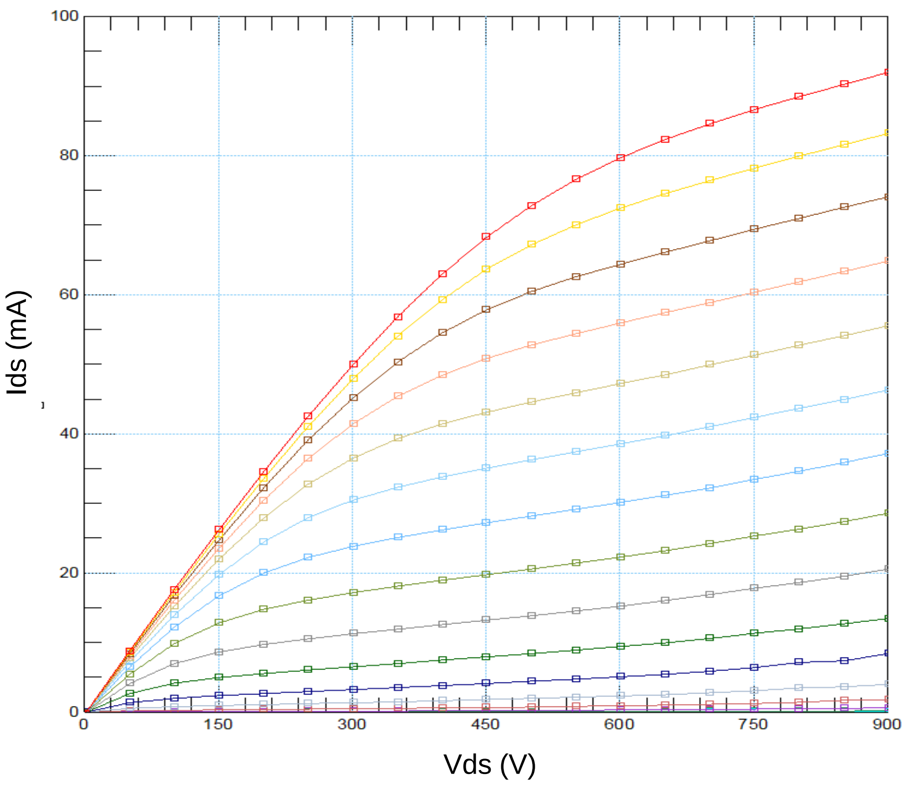


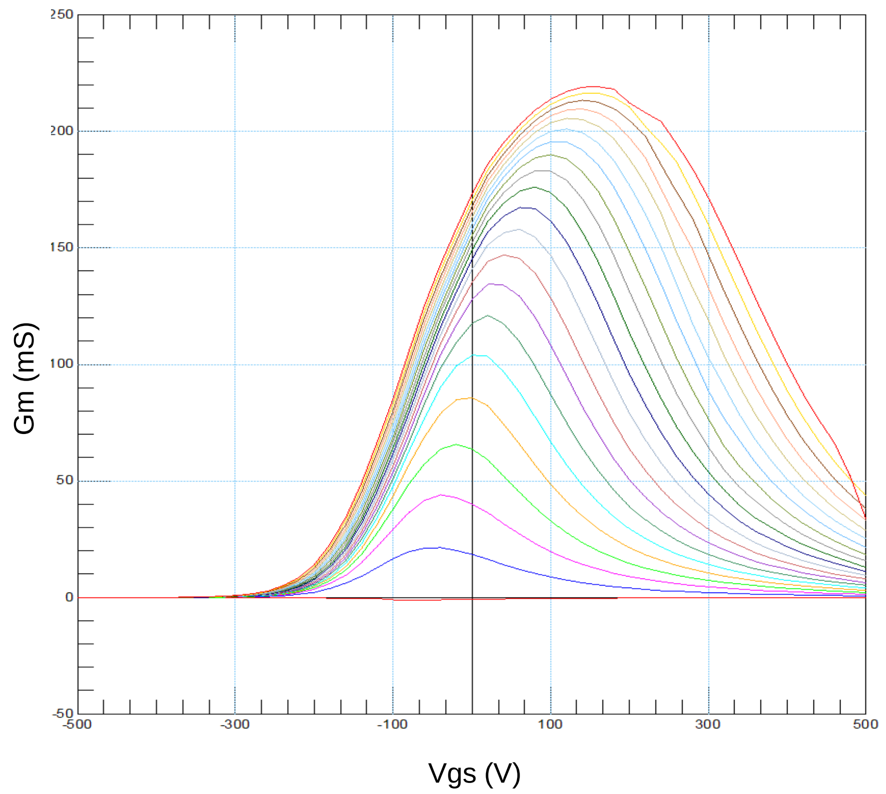


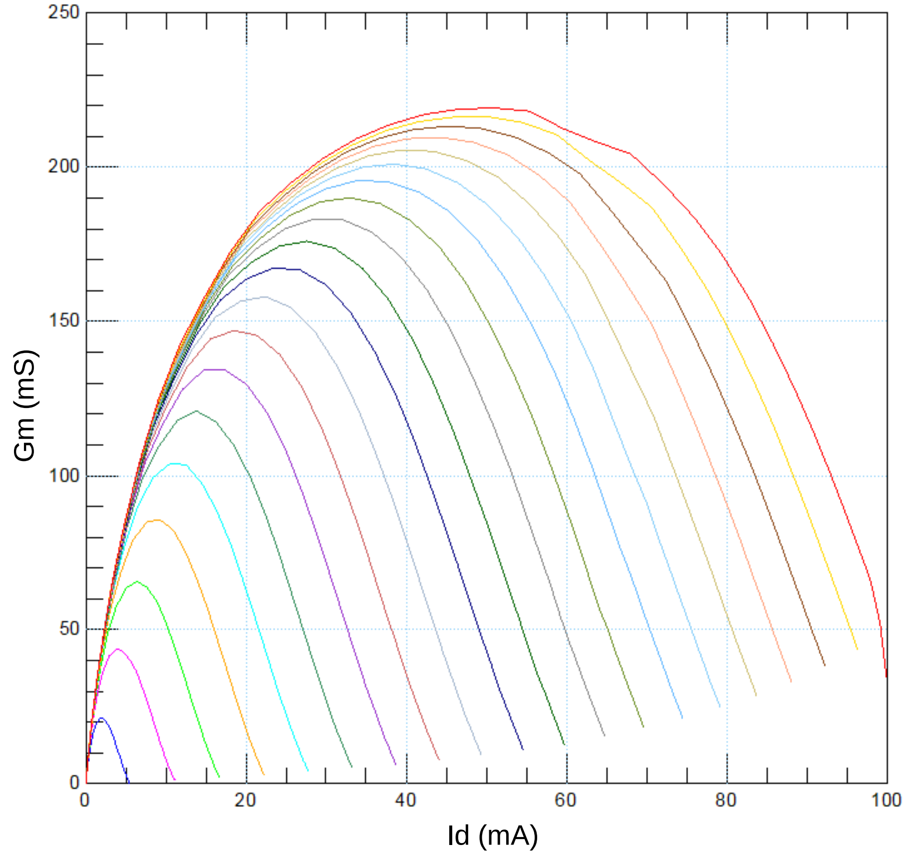


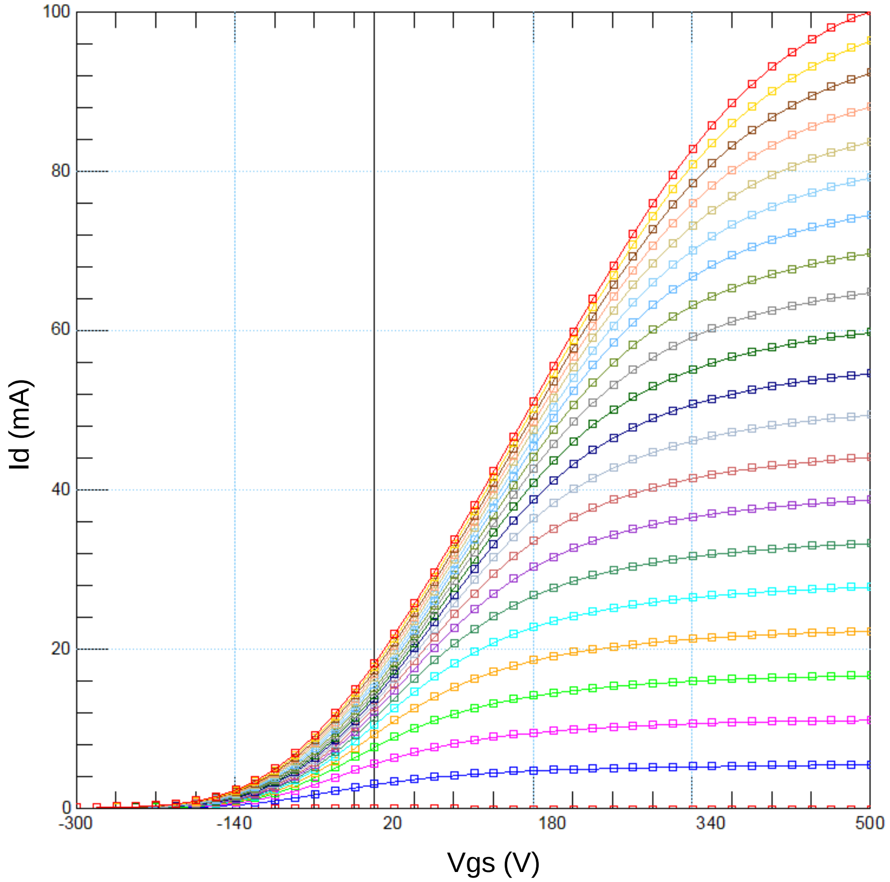


➢ D4F50 um transistor

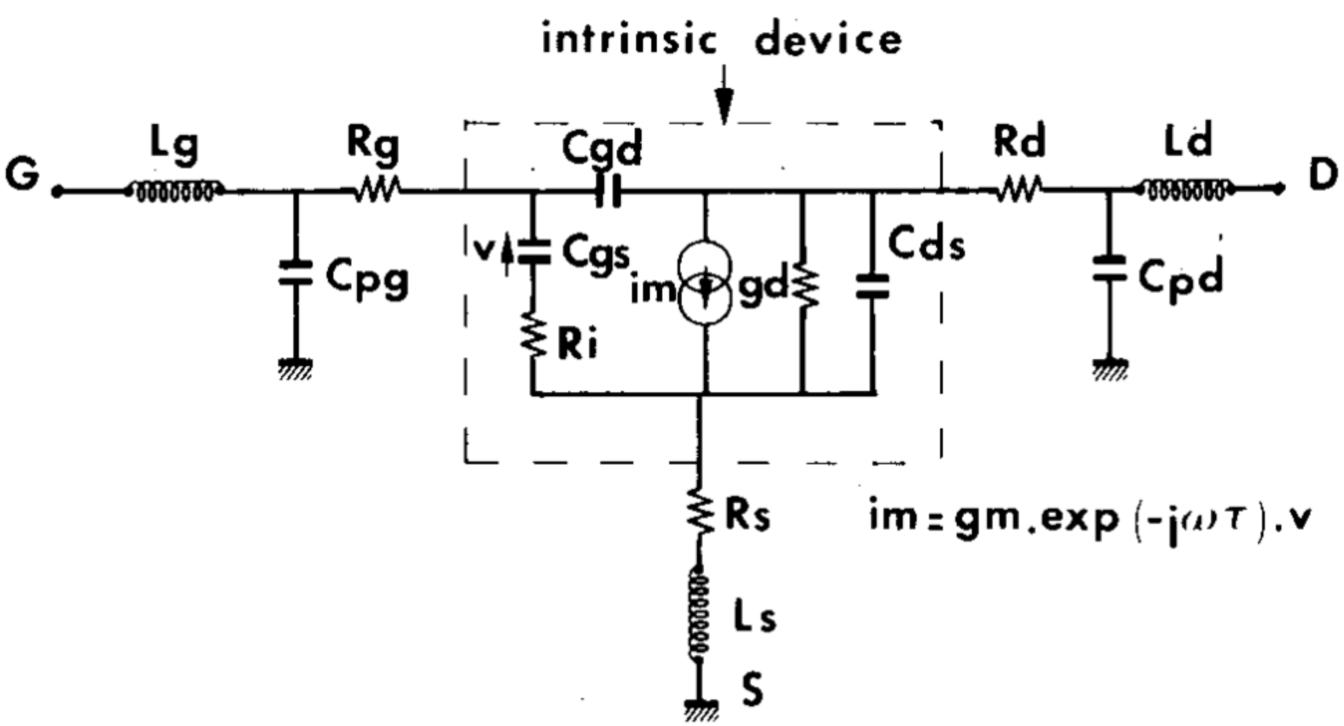




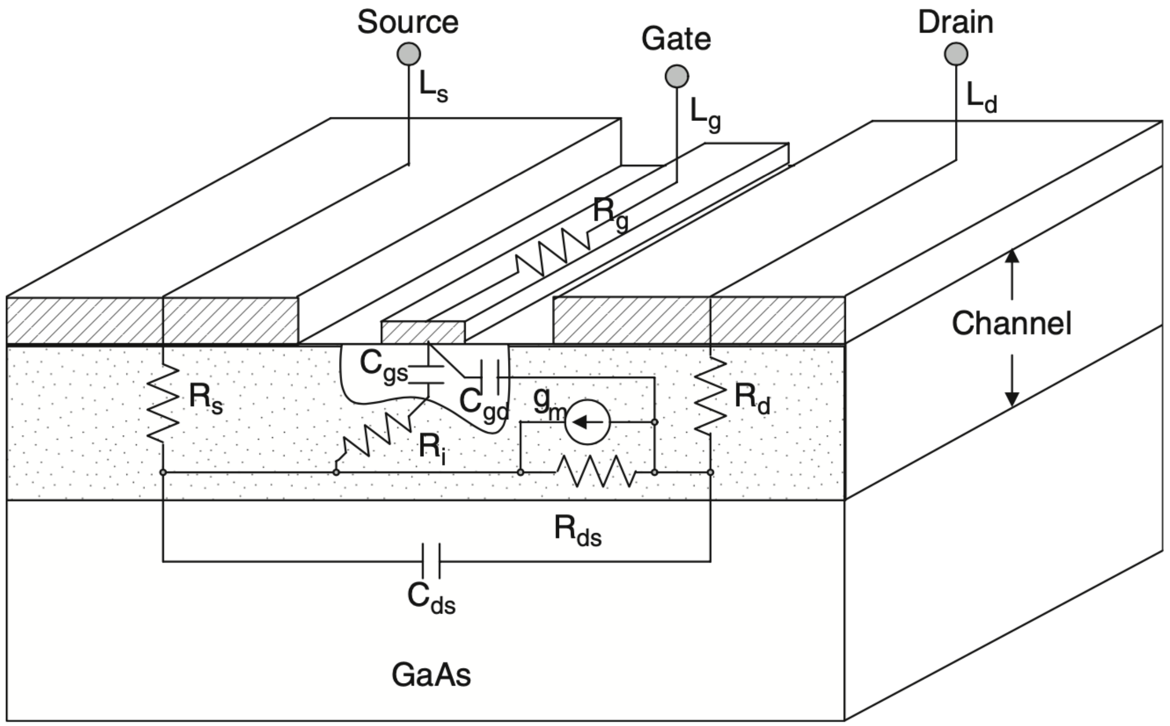




➢ *Small Signal Equivalent Circuit*



Small signal equivalent circuit of a field effect transistor. Gilles Dambrine, 1998



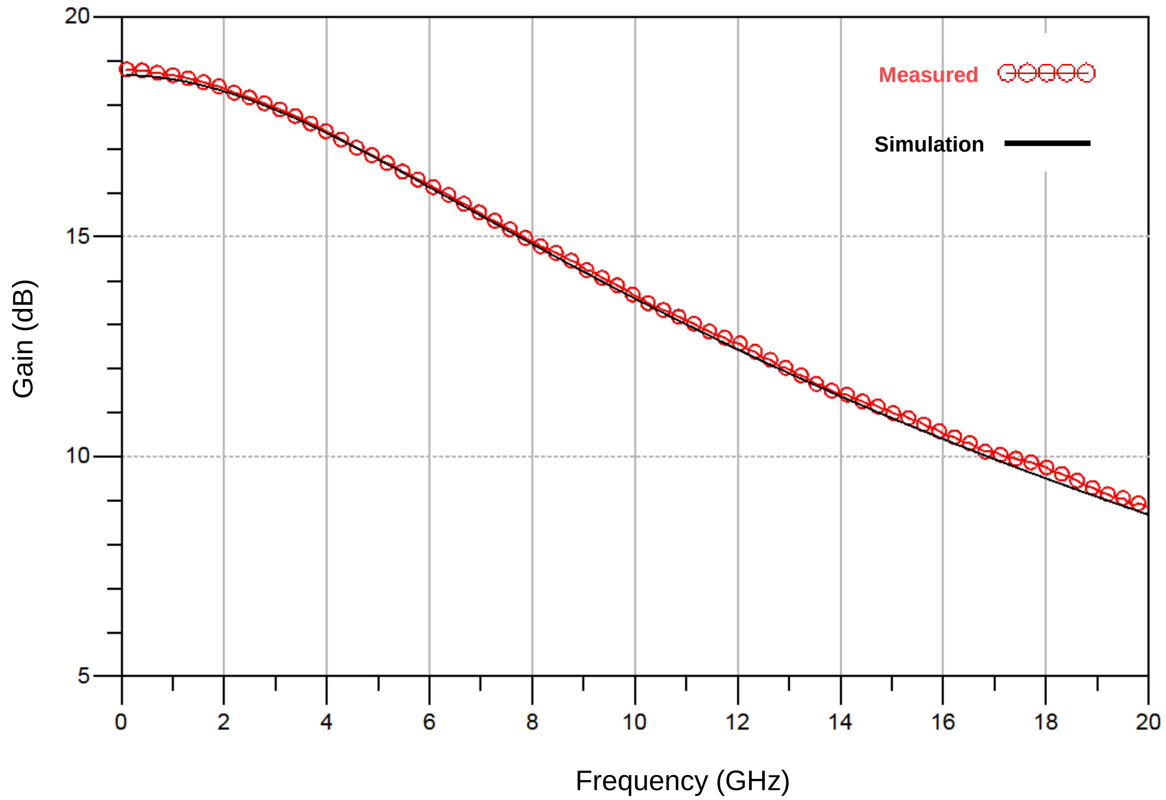
Small-signal equivalent circuit of a MESFET and the physical origin of the circuit element. Inder J.Bahl, 2009

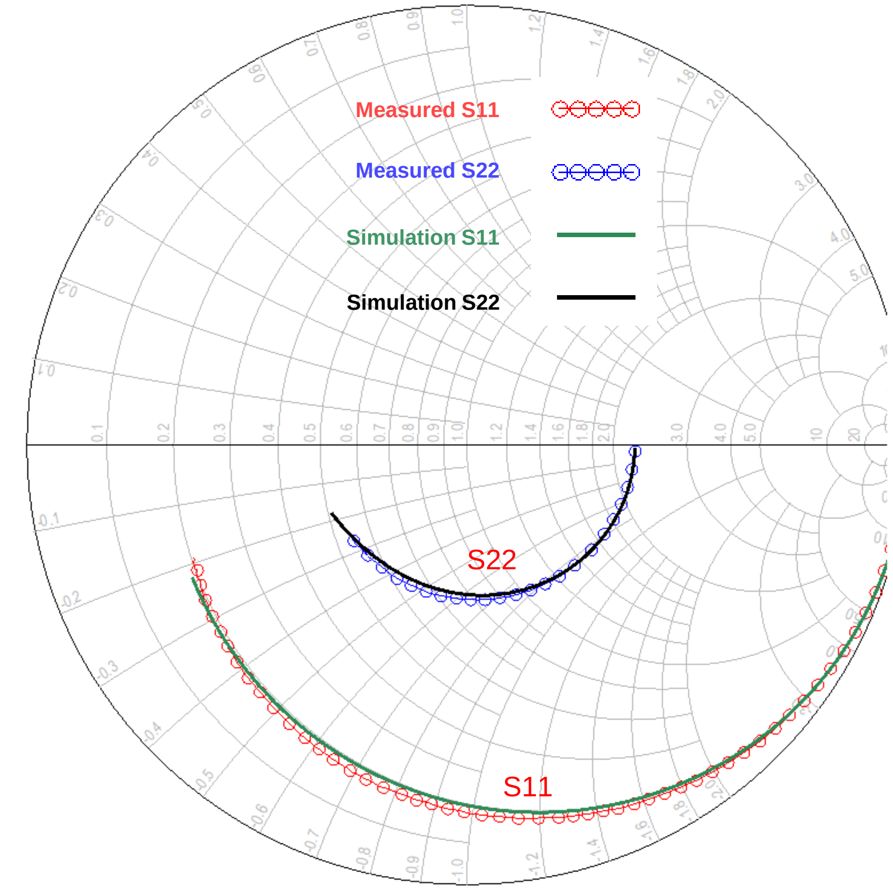
- **Rg, Rs and Rd: three-terminal pad resistance**
- **Ld, Ls and L: three-terminal pad inductance**
- **Cpg and Cpd: gate and drain pad capacitance**

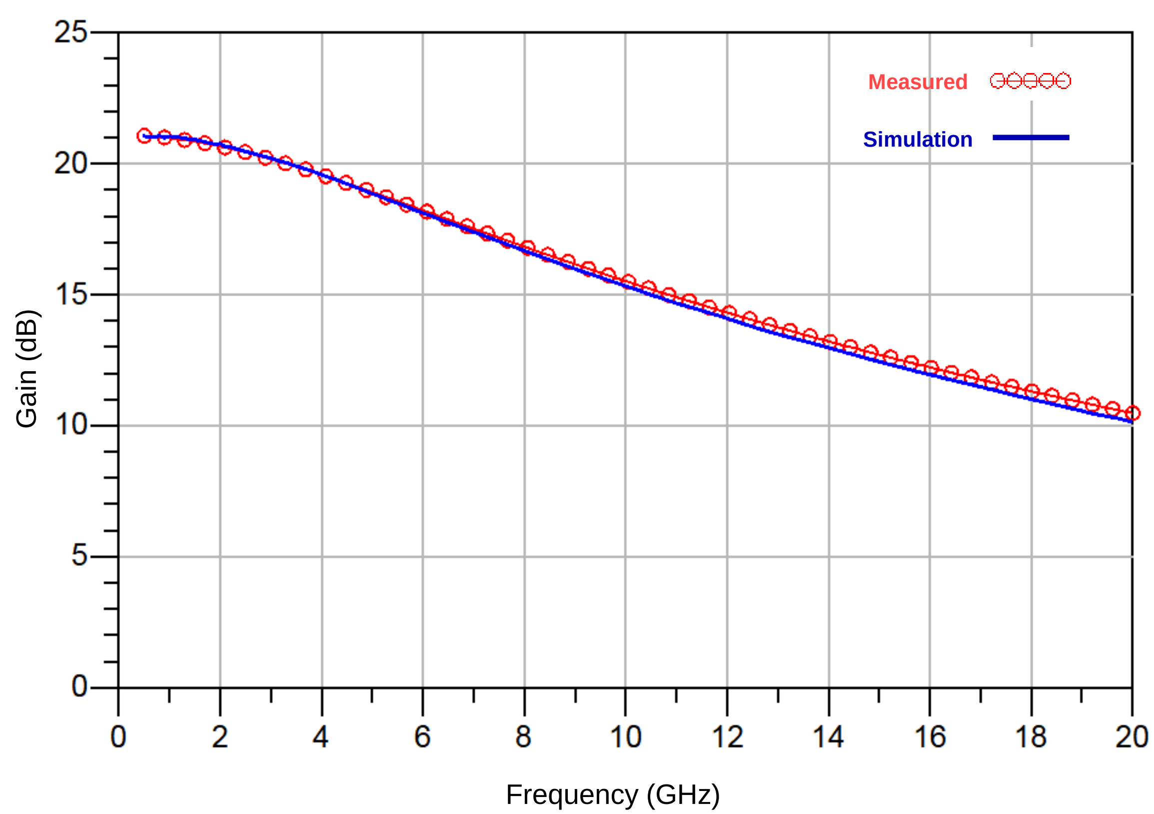
Extrinsic elements

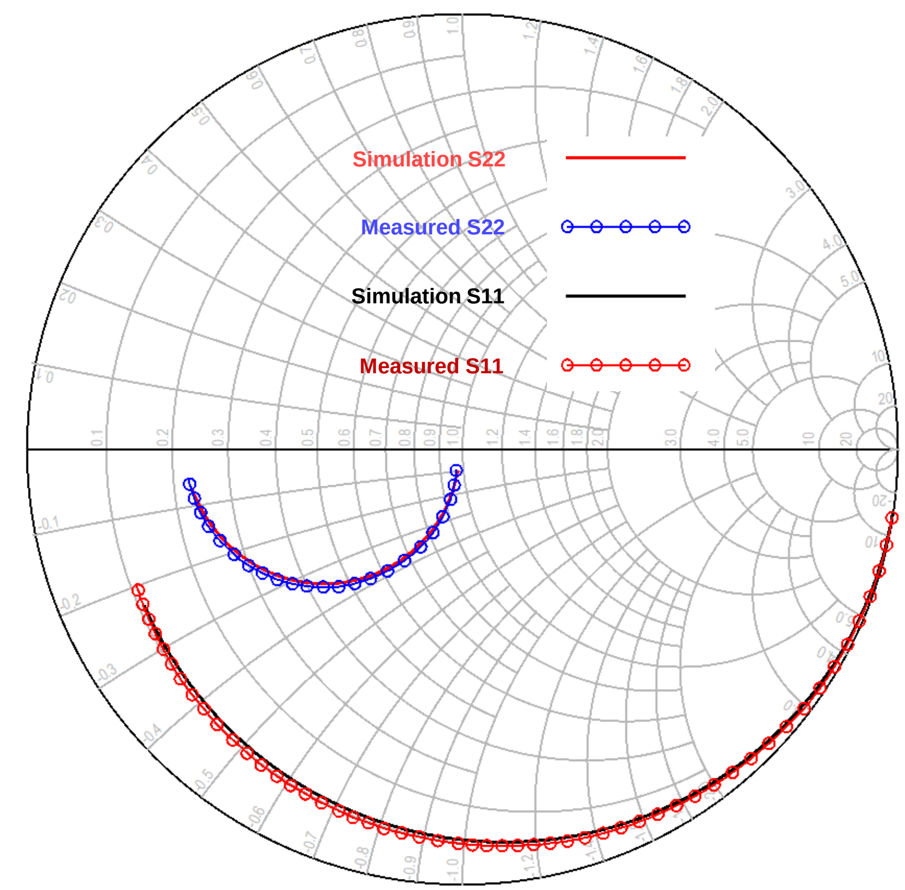
- **Cgs: gate to source capacitance**
- **Cgd: feedback capacitance**
- **Ri: gate to source resistance**
- **Rds: drain to source resistance**
- **Tau: delay time**

Intrinsic elements

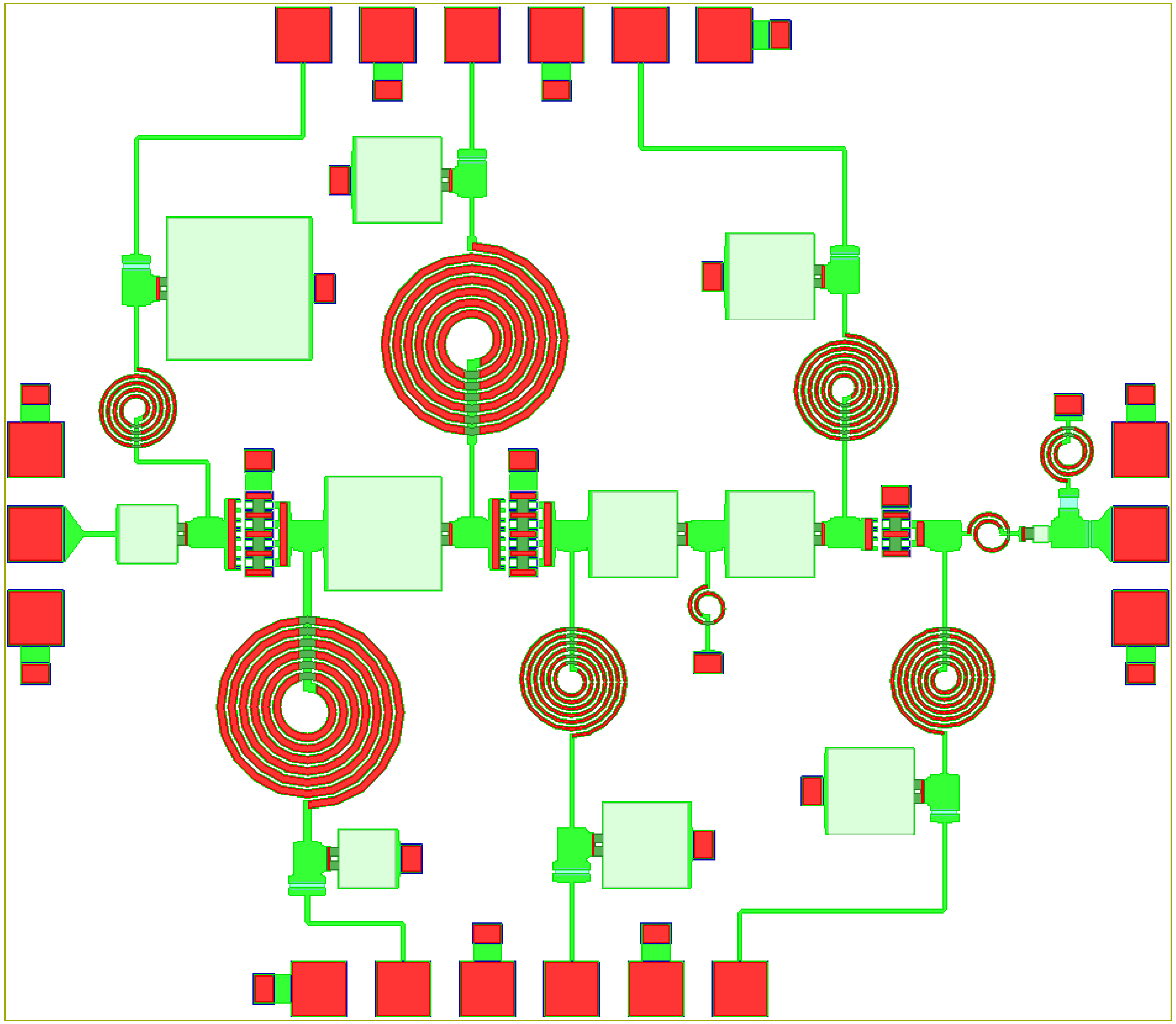

Measured
Simulation
Gain (dB)
Frequency (GHz)
20
15
10
5
0
2
4
6
8
10
12
14
16
18
20


Measured S11
Measured S22
Simulation S11
Simulation S22
S22
S11

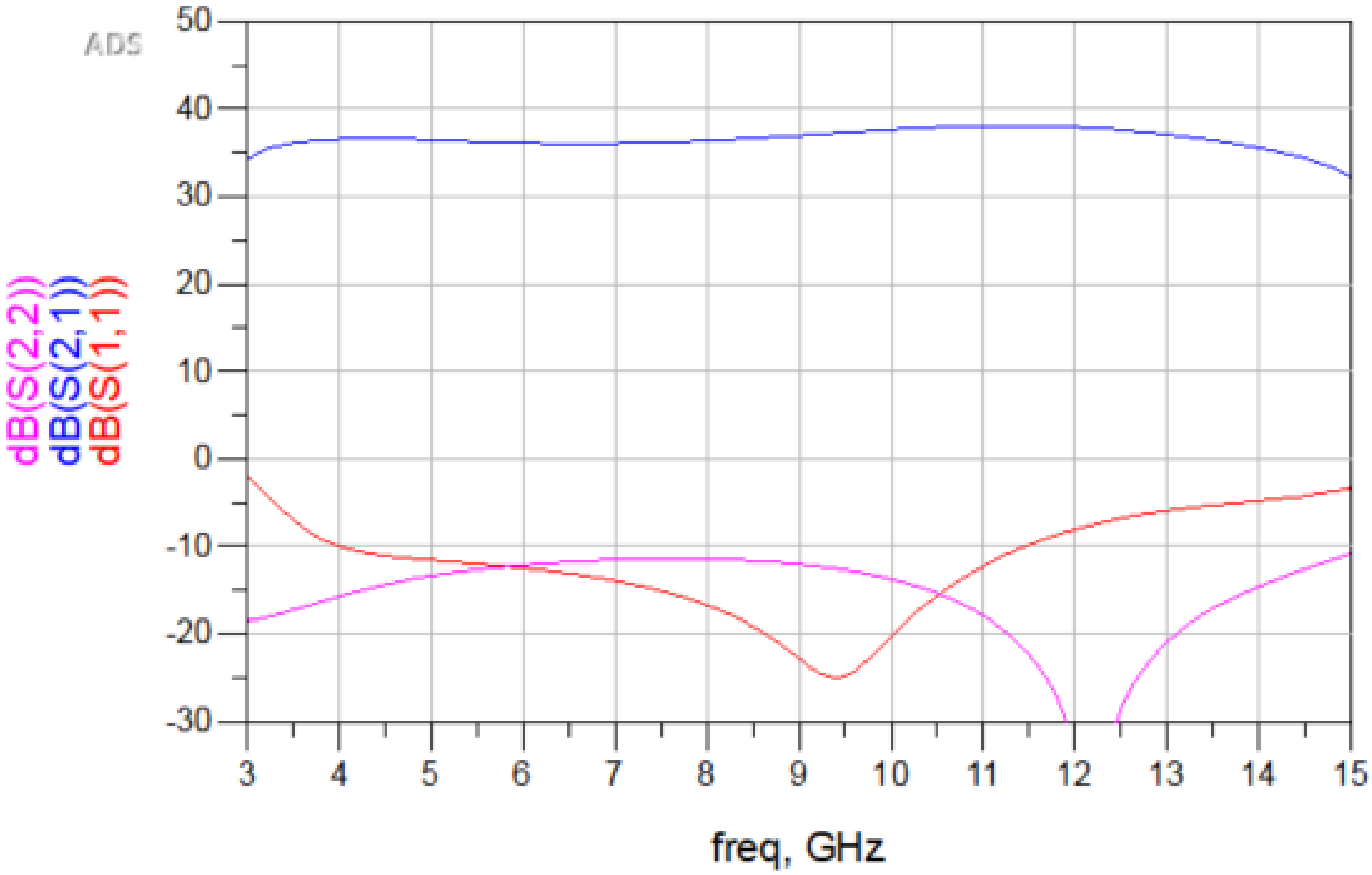

Measured
Simulation
Gain (dB)
Frequency (GHz)
25
20
15
10
5
0
0
2
4
6
8
10
12
14
16
18
20


Simulation S22
Measured S22
Simulation S11
Measured S11

4. A 4 - 14 GHz MMIC LNA Design

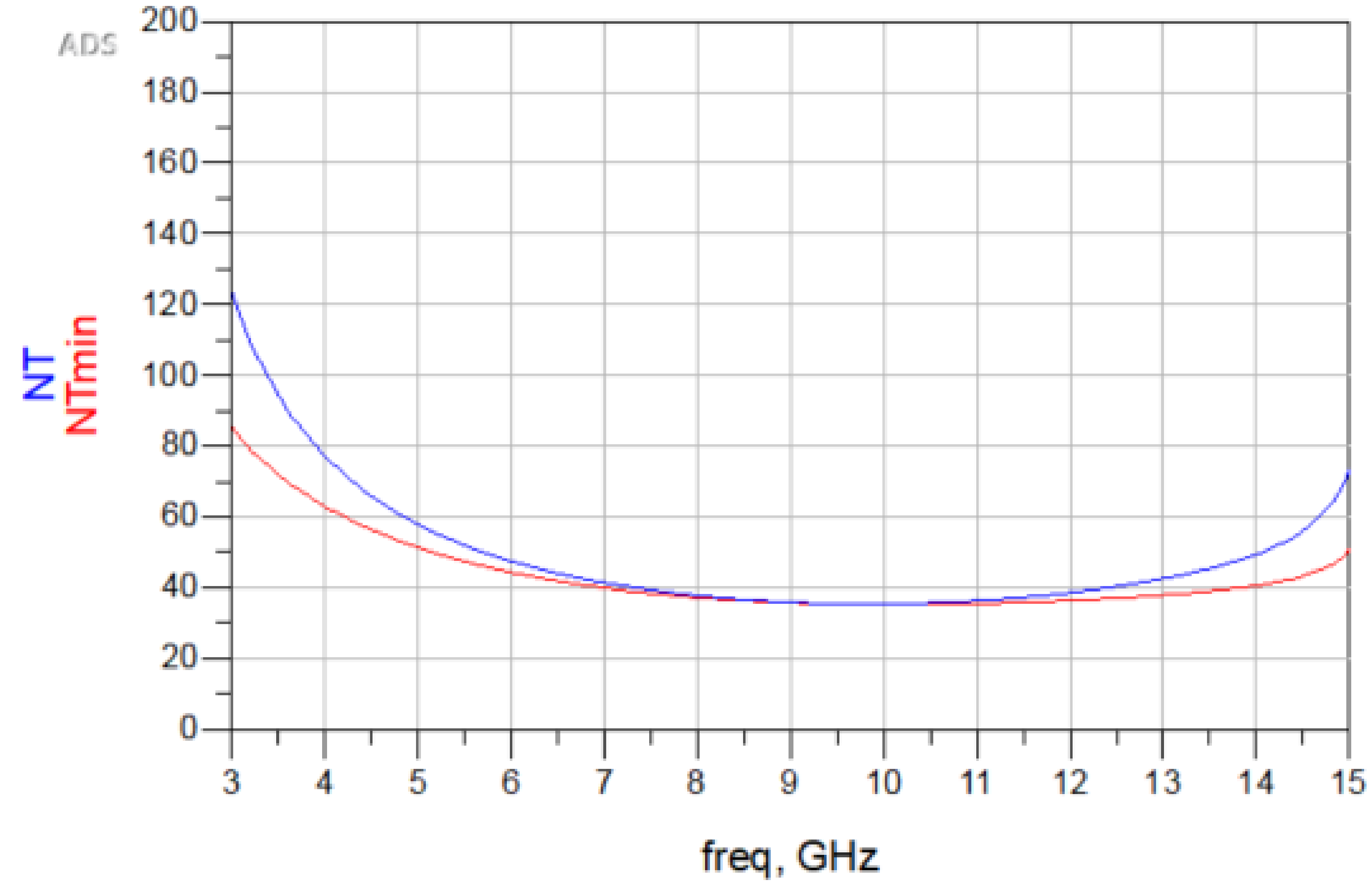


- WIN PP10-10 Technology
- Three stages MMIC LNA with Two 8 x100 um and one 4x100 um transistors
- Size: 2.01mm * 1.80mm



- **Gain: > 35 dB**

- **Noise temperature: 36 K (20 % bandwidth) and under 40 K (50 % bandwidth)**



5. Future Work

1. Characterisation WIN and Diramics transistors while a gradient temperature changes from 4 K to 290 K. WIN’s transistors include PP10-10 and PP10-20 technology.

2. Developing noise measurement system and extraction transistors’ noise model from 4 K to 290 K environment.

3. WIN PP10-20 pHEMT transistors characterisation and modelling

4. LNAs design for radio telescope: MMIC LNAs designed using WIN technology and discrete LNAs designed using Diramics transistors.

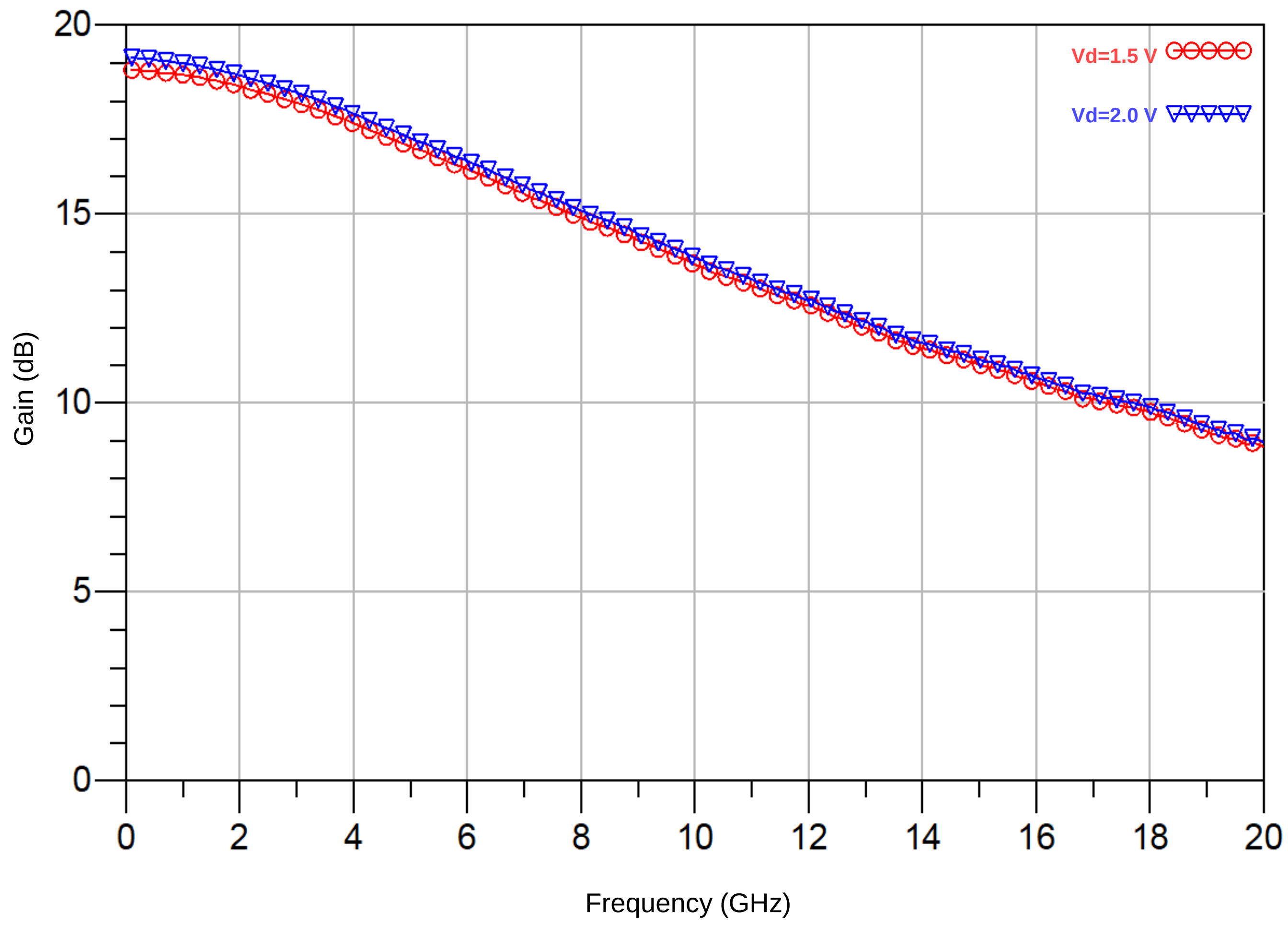
Thank you!

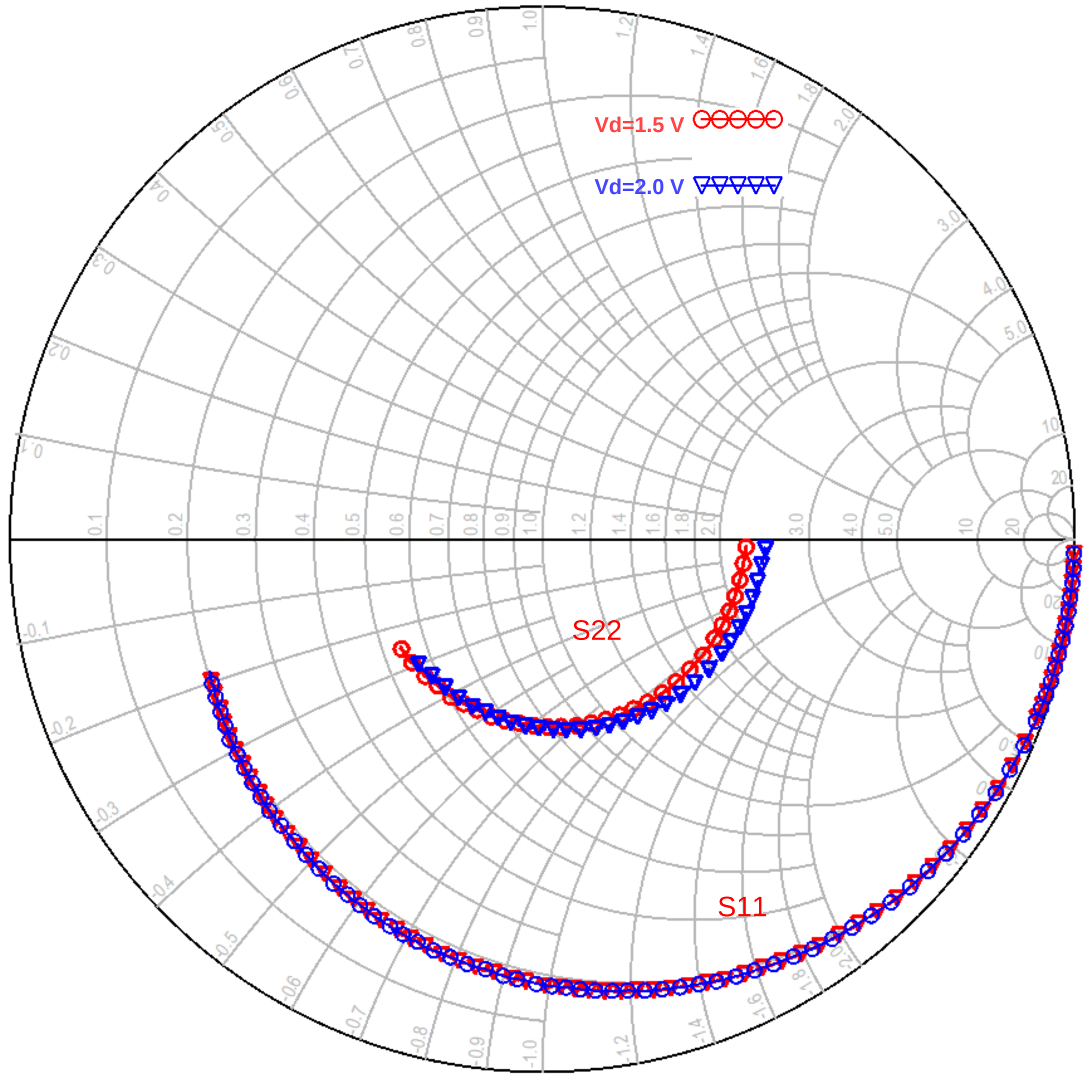
Any questions?

APPENDIX

➢ *S parameters measurement result*

- **Unbiased condition: Vds = Vgs = 0 V**
- **Pinched condition: Vgs = -1.0 V, Vds = 0 V**
- **Biased condition: Vgs = -0.5 V Vds = 1.5 V and 2.0 V**
- **Frequency range: 0.1 ~ 20 GHz**





➢ *S parameters measurement result*

- **Unbiased condition: Vds = Vgs = 0 V**
- **Pinched condition: Vgs = -0.4 V, Vds = 0 V**
- **Biased condition: Vds = 0.6 V, Vgs = 0, 0.05, 0.1, 0.15 and 0.20 V**
- **Frequency range: 0.1 ~ 20 GHz**