

Phased Array Receiver Prototype for TNRT

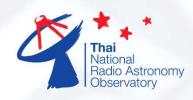
By

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- 1. Project Introduction & Objectives
- 2. Scope
- 3. Concept design
- 4. Conclusion



Source: APERTIF PAF, Westerbork Synthesis Radio Telescope, ASTRON, Netherlands

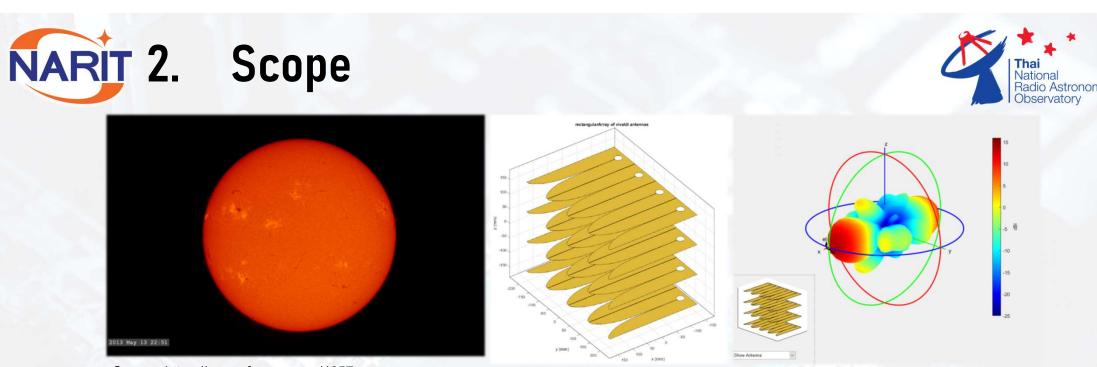
TNRT, Chiang mai, Thailand

- This project is proposed to do the "Phased array receiver protype" for TNRT.
- Study and research on designed know-how preparing the development for TNRT.
- Plan for 3 years, FY2022 2024:

Concept design → Implement to system → Observe (test)

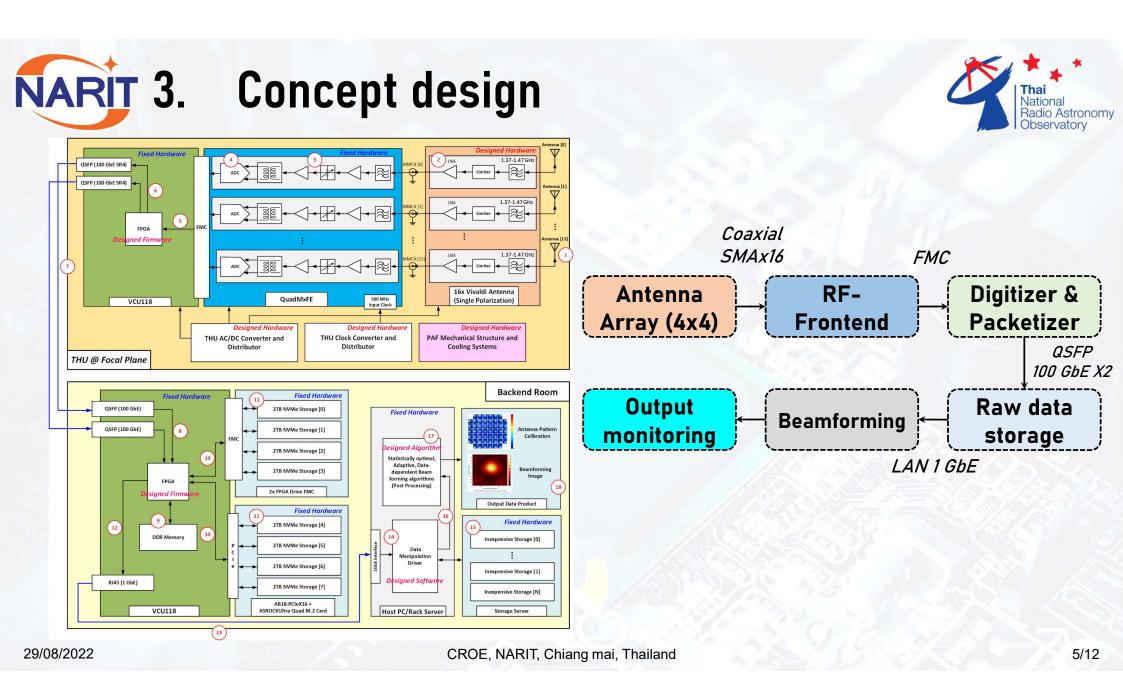
 Increasing Field of View of TNRT by using beam steering technique for Sky survey, on next phase of TNRT's receiver development.

CROE, NARIT, Chiang mai, Thailand



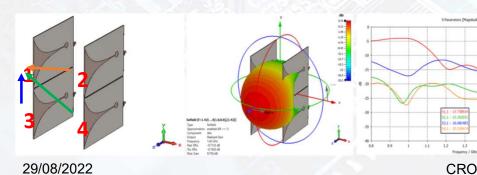
Source: https://svs.gsfc.nasa.gov/4657

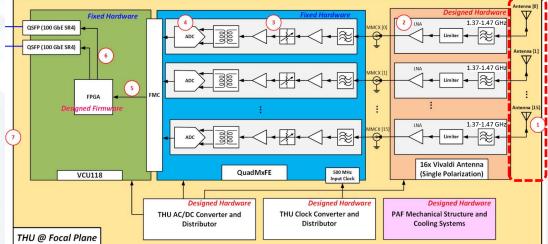
- Create for Sun tracking application by Hydrogen line (HL)
- Center frequency at 1.42 GHz, Neutral Hydrogen's frequency
- Phased array antenna size = 4 x 4 = 16 elements, with single polarization
- Digital Beamforming
- Output data format: Data cube (time/frequency/magnitude)

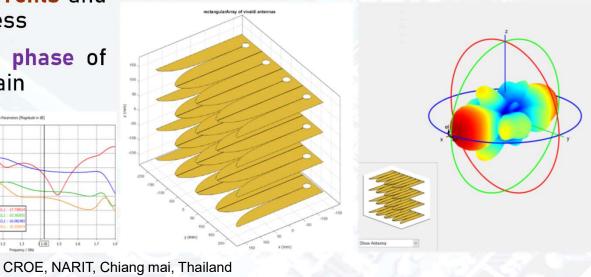


i. Antenna Array

- Center frequency 1.42 GHz
- Operating frequency 1.37-1.47 GHz (100 MHz of bandwidth)
- Size 4 x 4 , total 16 elements with single polarization
- Each element is Vivaldi antenna
- Convert RF signal
 → Electric currents and feed to RF chain for further process
- Each antenna receives different phase of RF signal with same offset and gain

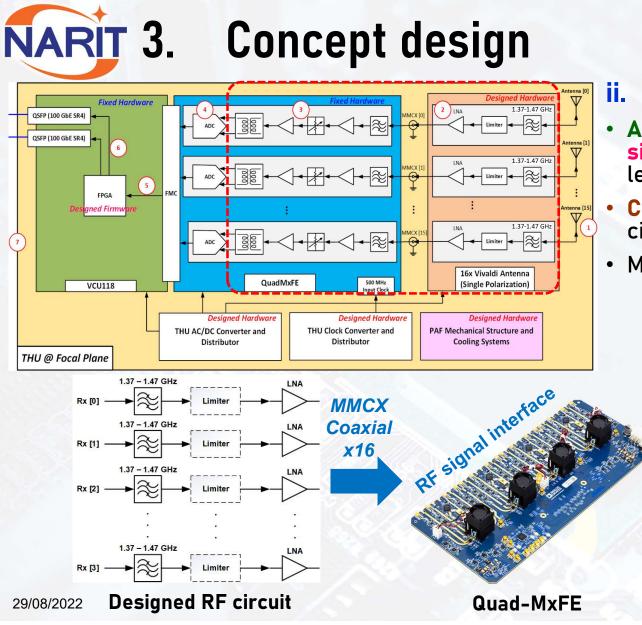


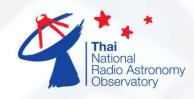




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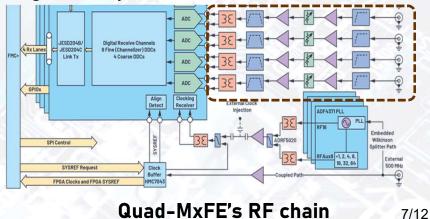
Radio Astronomy Observatory





. RF-Frontend

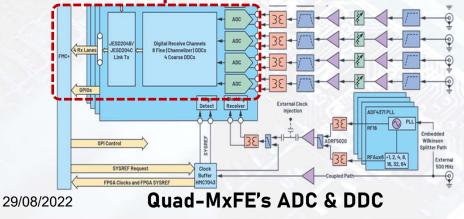
- Allow passband signal, improve quality of signal, such as SNR, signal gain, power level, etc.
- Composes with 2 stages: Designed RF circuit, Digitizer module (ADI's Quad-MxFE)
- Main components:
 - Bandpass filter
 - Limiter
 - Low Noise Amplifier
 - Digital Step Attenuator

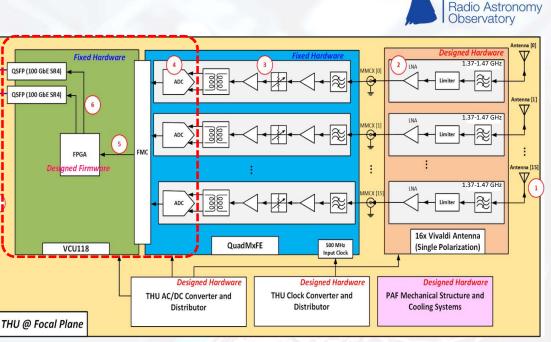


NARIT 3. Concept design

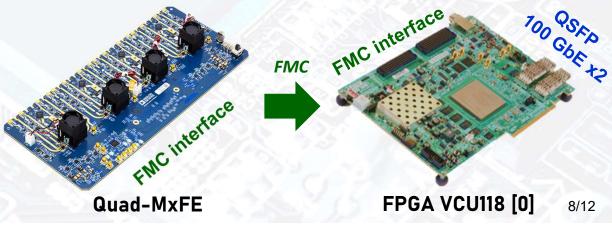


- Digitizer (Quad-MxFE):
 - ADC: sampling rate 4 GSPS, 12-bit x 16 channels
 - Digital Down Converter (DDCs): convert RF signal → baseband I/Q pair (sampling > 100 MHz x 32 channels)
- Packetizer (FPGA VCU118):
 - Add header & pack the I/Q data as payload of UDP protocol
 - Sent out UDP packets via 2x 100 GbE
 QSFP port



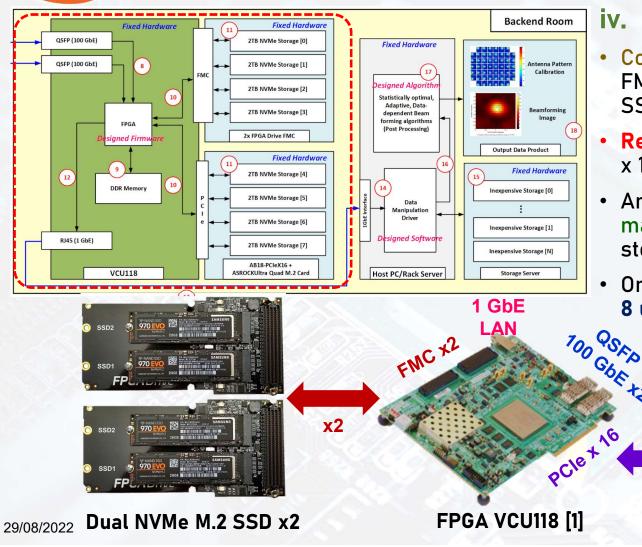


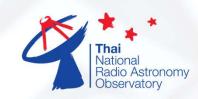
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NARIT 3.

Concept design





iv. Raw data storage

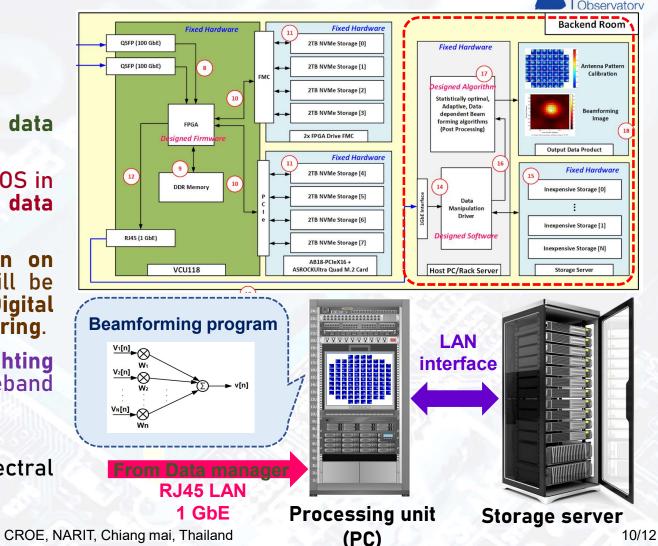
- Composes with 3 parts: FPGA Data manager, FMC Dual NVMe M.2 SSD, PCIe Quad NVMe M.2 SSD
- Record UDP packet data from Packetizer via 2 x 100 GbE QSFP
- Another FPGA VCU118 will be programmed to manage data (Write & Read) to/from memory storage
- On each 2 parts of memory storage, it includes 8 units x 2 TB NVMe M.2 SSD
- Data query from NVMe storages to the Beamforming processing unit via 1 GbE LAN over TCP/IP protocol.



NARIT 3. Concept design

v. Beamforming & Output monitoring

- Offline processing in software
- Request data query from FPGA data manager via 1 GbE LAN
- Digitized data will be backed up on OS in hard-disk RAID storage server for data protection.
- For this process, software design on program, e.g. python, MATLAB, will be designed to get data for Digital Beamforming algorithm and monitoring.
- Sub-band beamforming with weighting in frequency domain for wideband beamforming
- Output products:
 - Beamforming images: spectral result to spectrogram
- Antenna pattern synthesis



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• Activity list of FY2022:

☑ New RF antenna engineer: Dr. Nattapong Duangrit

☑ Concept design for prototype development

- ☑ Purchase all required equipment and materials for next year hand-on plan
- Start on Antenna design; simulation, fabrication, experiment plan

Plan for FY2023:

Recruit new software engineer for Beamforming & Output monitoring development

Implement concept design -> real prototype in laboratory scale

• Plan for FY2024:

Apply real prototype in laboratory scale to OTA test